

MULTI-VENDOR PCIe GEN6 RETIMER MANAGEMENT SUITE

Phoenix

One tool to bring up, validate, and qualify PCIe Gen6 retimers — across silicon vendors.

Phoenix discovers the part over sideband, exposes every on-chip instrument behind a single dashboard, API, and CLI, and produces the timestamped evidence your qualification report needs — from first scan to overnight soak.

WHY RETIMERS NEED THEIR OWN TOOL

Sideband-driven, capability-gated, qual-ready

A retimer sits in the channel where signal integrity is won or lost — but it has no host driver to lean on. Phoenix talks to it directly and adapts to exactly what each chip exposes.



Multi-vendor by design

One workflow for Broadcom Vantage (BCM85667) today, with Marvell Alaska-P (MV-CHP1016x) recognized and lighting up per feature as it validates — no separate tool per vendor.



Capability-gated UI

Phoenix shows only the pages and commands a chip actually advertises. Connect a part and you see exactly what it supports — no dead controls, no guessing.



Evidence in one call

Capture a timestamped, labeled artifact — status, FEC, recovery, eye, margin, ELA — in a single click or REST call. The bundle a qual record or interop cell needs.

CLEAN SCAN = CLEAN BRING-UP

Localize the problem before you touch protocol

Phoenix's detect → identify → load-profile flow is the first proof a board is powered, out of reset, clocked, and correctly wired. A device appears only when all three steps succeed — so a failed scan points straight at power, clock, wiring, or driver, not protocol debug.

64 GT/s

PCIe Gen6 retimer validation, PAM4-ready

5

On-chip instruments in one diagnostics workbench

3

Interfaces: Web dashboard, REST API & CLI

16

Lanes per port, both ports (PPA / PPB)

THE DIAGNOSTICS WORKBENCH

Five instruments, one signal-integrity surface

Phoenix gathers the retimer's on-chip SI and link-debug tools behind a single tabbed page — each answering one question a validation engineer asks at the bench.



PRBS

Generator / checker — "Is this lane error-free at the target rate?" Per-lane BER.



Eye Diagram

Internal RX-margin capture — "How much eye opening?" in mUI / mV margins.



ELA

Embedded logic analyzer — "Why won't the link train?" LTSSM + PIPE trace.



BELA

RX capture / trigger status — "Did a rate-transition event fire?" (preview).



LinkCAT

Channel analysis — "What is the channel insertion loss?" dB at symbol rate.



Capture Evidence

One labeled artifact ties every reading together — bulk-capture a full rack in one request.

BEYOND DIAGNOSTICS

Full lifecycle, from firmware to soak



Firmware update & register browser

Push firmware and read/dump any register block with annotated decode — full low-level control when you need it.



Continuous monitoring (soak)

Server-side poll loop survives a closed browser tab — catches link flapping, thermal drift, and slow error accumulation overnight.



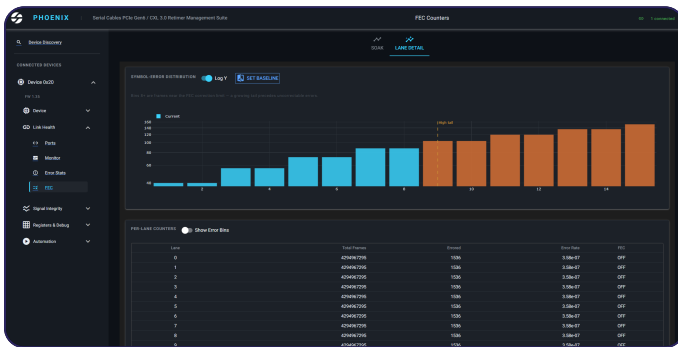
TX-EQ, SERDES & FEC counters

Tune transmit equalization, inspect CDR/DFE/AGC, and track Gen6 flit-FEC correctable/uncorrectable counters.



Recipes & workflows

Save a measurement sequence once and replay it identically on every DUT — by hand or driven from CI.



FEC counters — per-lane symbol-error distribution. Gen6 flit-FEC correctable/uncorrectable, charted and tabulated.



Device dashboard. Temperature, voltage rails, and per-port (PPA/PPB) link status at a glance.

MULTI-VENDOR SUPPORT

One tool, support that grows with your silicon

Phoenix gates features by capability, so each chip shows exactly what it advertises. Broadcom Vantage is the primary, hardware-validated target today; Marvell Alaska-P is recognized now and enables per feature as each is validated on hardware.

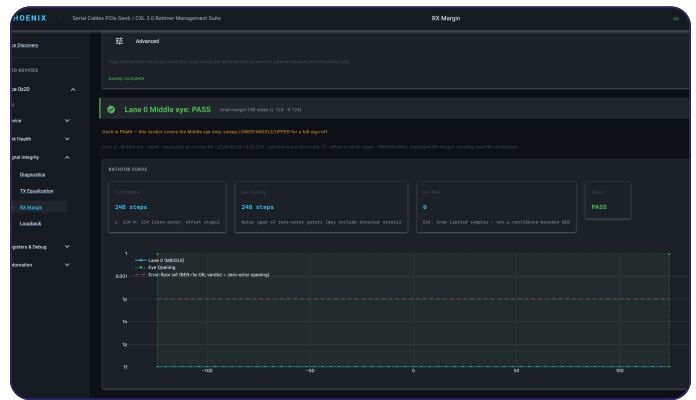
CAPABILITY	BROADCOM VANTAGE BCM85667	MARVELL ALASKA-P MV-CHP1016x
Device discovery & identification	Available	Identify only
Dashboard, port & link status	Available	Planned
PRBS, Eye diagram, ELA trace	Available	Planned
PCIe Lane Margining (§8.4.4)	Available	Vendor-specific — n/a
FEC counters (Gen6 flit FEC)	Available	Planned
TX-EQ, SERDES, Loopback	Available	Planned
Firmware, monitoring, recipes & workflows	Available	Planned

Legend: **Available** = hardware-validated · **Identify only** = recognized, measurement pages not yet enabled · **Planned** = enables as validated on hardware.

A SPEC FEATURE, NOT A VENDOR TRICK

Lane Margining at the Receiver (§8.4.4)

Lane Margining at the Receiver is a **PCIe-specification** capability: a standardized way for a receiver to report its own timing and voltage margin. Because the method is defined by the spec, results are obtained and interpreted the same way on any compliant receiver — which is why it matters for compliance reporting. It is available today on Broadcom Vantage.



Lane Margining at the Receiver — per-lane bathtub & PASS. Spec-defined timing/voltage margin (Broadcom Vantage).

BUILT TO SCRIPT

API & automation

Every measurement is reachable over a key-authenticated REST API (X-API-Key / PHOENIX_API_KEY), with a stable device-event WebSocket stream built for soaks and CI. Drive Phoenix from the dashboard at the bench, then run the identical sequence headless in your pipeline.

- WEB DASHBOARD
- REST API
- CLI
- WEBSOCKET STREAM

TWO READERS, ONE TOOL

Bench & lab, served together

Phoenix serves the operator driving the UI to get a task done *and* the PCIe Validation Engineer interpreting what each measurement means — pass/fail guidance, units, and what good versus bad looks like, on the same pages.

TALK TO US

Validate Gen6 retimers across every vendor

Serial Cables, LLC · Englewood, CO · Phoenix Retimer Manager for PCIe Gen6 signal-integrity validation. | serialcables.com