SERIAL CABLES

PCIe Gen6 MCIO Host Card

PEX90080-B0 Atlas III 64-lane Switch Chip

TECHNICAL MANUAL

Revision 1.1 May 2026

PCI6-AD-x16HI-BG6-80-B0

Quarch Ready

Command-line interface for monitoring

PCI EXPRESS 6.0

CXL Compute Express Link

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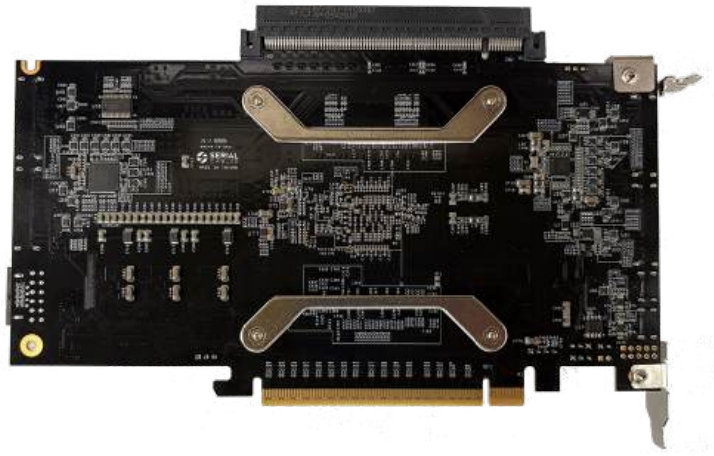
Product Overview

The Serial Cables Atlas3 B0 Host Adapter Card is a PCIe Gen6 switch-based platform designed for high-speed connectivity, validation, and system integration. Built around the Broadcom Atlas3 PEX90080 switch, the card enables flexible PCIe fanout across multiple downstream devices using MCIO and straddle-mounted interfaces.

This adapter provides up to 64 lanes of PCIe Gen6 connectivity through four MCIO x8 connectors and one PCIe x16 straddle connector. It allows engineers to connect, test, and scale next-generation PCIe devices—including NVMe SSDs, accelerators, and expansion boards—without requiring native Gen6 host platforms.

An onboard microcontroller (MCU), accessible through USB Type-C, enables direct command-line control for configuration, monitoring, and firmware management. The platform supports both managed and unmanaged firmware modes, offering flexibility for low-level hardware validation as well as higher-level system control.



Key Features

- **Broadcom Atlas3 PCIe Gen6 Switch (PEX90080)** — Up to 80 lanes and 40 ports across five x16 stations.
- **64 Lanes of Gen6 Connectivity** — Four right-angle MCIO x8 (SFF-TA-1016) connectors plus one PCIe Gen6 x16 straddle-mount connector.
- **Dual Power Input Support** — Supports PCIe slot power or CN8 12V 2×6 auxiliary power for higher-load configurations.
- **Integrated MCU Control** — CN7 USB-C access for CLI management, diagnostics, and firmware updates.
- **Onboard Diagnostics** — CLI access to temperature, voltage, fan speed, power, link status, counters, and I²C checks.
- **Flexible Port Modes** — Supports managed/unmanaged firmware, dynamic port configuration, NT ports, DMA channels, and peer-to-peer transfer.

Safety, Handling, and Compliance

The Atlas3 B0 Host Adapter Card is intended for use in controlled environments such as server systems, test platforms, and engineering labs. Installation and operation should be performed by personnel familiar with high-speed PCIe systems and ESD-safe handling practices.

Improper installation, insufficient power delivery, or inadequate cooling may result in degraded performance or hardware failure.

Electrical Safety

The host adapter card can draw power from two sources:

- **PCIe edge connector (golden finger)**
- **Auxiliary 12V 2×6 EPS connector (CN8)**

The auxiliary connector provides additional power for the switch, cooling system, and downstream PCIe devices, including up to 75W for the straddle connector.

Before installation:

- Power down the host system and disconnect all AC sources.
- Verify sufficient 12V rail capacity for the host card and connected devices.
- Do not connect or disconnect MCIO cables, straddle connectors, or power leads while the system is energized.
- Always connect auxiliary power before system startup when using the straddle interface.

Failure to provide adequate 12 V capacity can overstress the slot regulator or cause switch malfunction.

ESD Protection

This device contains components sensitive to electrostatic discharge:

- Work only in an electrostatic discharge-safe area with a grounded mat and wrist strap.
- Keep the card in its anti-static packaging until you are ready to install it.
- Avoid touching connector pins, exposed traces, or any metallic contacts.

Thermal and Airflow Considerations

The board includes an active heatsink and blower assembly and requires proper airflow for stable operation:

- Maintain clear airflow around the card and its heatsink.
- Do not block nearby fans or obstruct ventilation inside the chassis.
- Operate the adapter only within an ambient temperature range of 0 °C to +40 °C.

Compliance

This product is manufactured in accordance with standard international safety and environmental regulations:

- **CE** – Conforms to applicable European EMC and low-voltage directives.
- **FCC Class A** – Intended for use in commercial or industrial environments.
- **RoHS 3** – Compliant with the Restriction of Hazardous Substances directive.

Hardware Specifications

The Atlas3 B0 Host Adapter Card is a Gen6 x16 PCIe switch board that provides 64 lanes of Gen6 PCIe connectivity through four MCIO x8 connectors and one x16 straddle-mount connector. It is based on the **Broadcom Atlas3 PEX90080 switch**, which supports up to **80 lanes and 40 ports across five x16 stations** for flexible storage, expansion, and PCIe fanout configurations.

An onboard MCU provides management and diagnostic access through the card's USB Type-C interfaces. It communicates with the Atlas3 switch, power circuitry, thermal sensors, fan controls, and I²C devices, enabling CLI-based configuration, monitoring, firmware upgrades, and board-level diagnostics.

Parameter	Specification
PCIe Interface	PCIe Gen6 x16 edge connector and straddle connector
Switch Device	Broadcom PEX90080 Atlas3 PCIe Gen6 Switch
Total PCIe Lanes	80 lanes total across five stations (x16 each)
Active Ports on this Card	4 × MCIO x8 (SFF-TA-1016) + 1 × x16 straddle connector
Operating Voltage	12 V nominal (via PCIe slot and CN8 2×6 EPS connector)
Typical Power Consumption	~60 W to 80 W (board only, workload dependent)
Max Power Requirement	Up to 81 W (not including the power supply to straddle PCIe connector)
PCIe Slot Power	75W maximum (per PCIe specification)
Supplemental Power Input	12 V 2×6 EPS connector (CN8)
Operating Temperature	0 °C to +40 °C ambient
PCB Dimensions	209 mm (L) × 136 mm (H) × 44 mm (T) (including heatsink and blower)

Power Requirements

The Atlas3 B0 Host Adapter Card supports dual power input modes:

- PCIe slot only (limited use cases)
- **Auxiliary 12V 2×6 EPS connector (recommended)**

Using the auxiliary connector:

- Provides full power to the switch and cooling system
- Enables 75W delivery to the PCIe straddle interface
- Supports stable operation under high load conditions

Connector Locations and Functions

The Atlas3 B0 host adapter includes 8 primary connectors. All designators are silk-screened on the PCB.

Designator	Connector Type	Function / Description
CN1	PCIe Gen6 x16 Straddle-Mount Connector	Provides one x16 Gen6 link for riser or edge-based applications. Supports straddle-port power when CN8 is connected.
CN2 - CN5	Right-Angle MCIO x8 (SFF-TA-1016)	Four x8 MCIO ports for downstream PCIe devices, including sideband signals for reset, clock, and I²C.
CN6	USB Type-C Connector	Provides SDB and SMART UART access for debug and firmware-supported control.
CN7	USB Type-C Connector	Primary MCU control port used for CLI access, configuration, and firmware updates.
CN8	12 V EPS 2×6 Power Connector	Auxiliary 12 V input for the host card, cooling assembly, and straddle-port power.

CN1 – PCIe Gen6 Straddle Connector

CN1 provides one PCIe Gen6 x16 straddle-mount connection for edge-based, riser, or expansion-board applications. When CN8 auxiliary power is connected, the card can also provide power to the attached straddle-side device.

CN2 / CN3 / CN4 / CN5 – Right-Angle Type MCIO x8 Connectors

The four MCIO ports provide high-speed PCIe connectivity between the Atlas3 switch and downstream devices such as SSDs, JBOF systems, interposer cables, and PCIe expansion boards.

Each MCIO x8 connector supports:

- **4x PCIe HCSL reference clock outputs** on pins A8/A9, A11/A12, A26/A27, and A29/A30.
- **2x dedicated I²C interfaces** on pins B8/B9 and B26/B27 for management and control.
- **4x PERST# (PCIe Reset) signals** on pins B11/B12/B29/B30 to reset attached devices.

PCIe Lane Mapping

The MCIO connectors on the Atlas3 B0 host card are assigned specific groups of PCIe lanes from the switch:

- **CN2** – PCIe Lanes [7:0]
- **CN4** – PCIe Lanes [15:8]
- **CN3** – PCIe Lanes [39:32]
- **CN5** – PCIe Lanes [47:40]

Each connector carries eight PCIe differential pairs (x8 width) along with clock, reset, and management sideband signals.

For example, the following table shows the pinout for MCIO connector CN2, which carries PCIe lanes [7:0]:

CN2		2	3	5	6	8	9
	A B	PERN7 PETN7	PERP7 PETP7	PERP6 PETP6	PERN6 PETN6	MCIO_CLKA_PO MCIO_SCL_A0	MCIO_CLKA_NO MCIO_SDA_A0
		14	15	17	18	11	12
	A B	PERN5 PETN5	PERP5 PETP5	PERP4 PETP4	PERN4 PETN4	MCIO_CLKA_P1 MCIO_PERST#_A0	MCIO_CLKA_N1 MCIO_PERST#_A1
		20	21	23	24	26	27
	A B	PERN3 PETN3	PERP3 PETP3	PERP2 PETP2	PERN2 PETN2	MCIO_CLKA_PO MCIO_SCL_A0	MCIO_CLKB_NO MCIO_HDA_A0
		32	33	35	36	29	30
	A B	PERN1 PETN1	PERP1 PETP1	PERP0 PETP0	PERN0 PETN0	MCIO_CLKB_P1 MCIO_PERST#_B0	MCIO_CLKB_N1 MCIO_PERST_B1

CN6 – USB Type-C Connector (SMART UART)

The CN6 USB Type-C connector provides access to the Atlas3 SDB and SMART UART paths. These interfaces are used for low-level debug access and firmware-supported UART communication.

When connected to a PC, CN6 exposes two USB serial interfaces:

Port	Function	Notes
USB Serial Interface 1	Atlas3 I²C slave interface	Requires managed firmware support.
USB Serial Interface 2	SDB or SMART UART path	Can be switched between Atlas3 SDB and SMART UART. SMART UART requires managed firmware support.

CN7 – USB Type-C Connector (CLI)

The CN7 USB Type-C connector provides direct access to the onboard MCU. This is the primary management interface for CLI commands used to configure the Atlas3 switch, monitor board status, perform diagnostics, and update firmware.

For detailed descriptions of all supported commands, see **CLI Command Reference** and **Command Usage Notes**.

CN9 – Power Connector

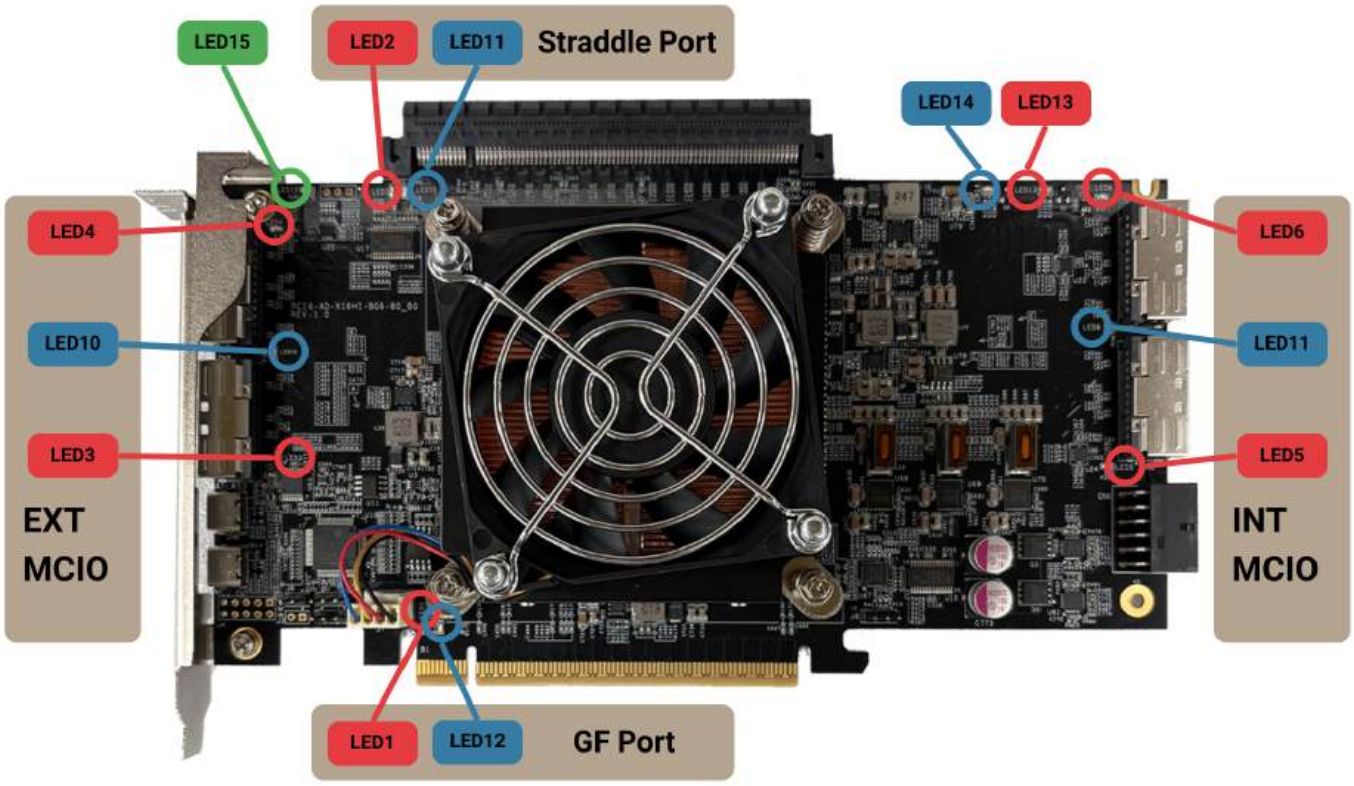
The CN8 connector supplies auxiliary 12 V power to the Atlas3 B0 host adapter. It uses a PCIe 2×6 power interface to provide power for the Atlas3 switch, the fan-sink cooling assembly, and the PCIe straddle connector (75W).

The pinout provides separate power, ground, and control signals:

Pin	Signal
1 – 6	+12V Power Input
7 – 12	Ground
S1	CARD_PWR_STABLE
S2	CARD_CBL_PRES#
S3	SENSE0
S4	SENSE1

LED Indicators

Status LEDs on the Atlas3 B0 board provide visual feedback for system faults, firmware state, MCU activity, and PCIe link speed.



System Status LEDs

LED ID	Color	Description
LED13	Red	**System Error Indicator.** Turns on for: • Second expiration of the watchdog timer. • Built-In Self-Repair (BISR) fault detected. • IBR firmware reported a signature authentication failure. • Double-bit ECC error detected during IBR read operations. • Other conditions classified as fatal errors.
LED14	Green	**Atlas3 Heartbeat.** Blinking indicates the managed firmware is running normally. Solid on indicates unmanaged mode.
LED15	Green	**MCU Status.** Blinking shows the MCU firmware is active and responding.

Link Speed LEDs

The Link Speed LEDs (blue) indicate the active PCIe generation for each connected port, providing a quick visual reference for link status and performance.

- If a link is inactive, its LED remains off. For example, if the first EXT MCIO port group links at Gen6, LED10 turns on to indicate Gen6 operation.
- When multiple ports on the same connector operate at different generations, the LED reflects the highest negotiated speed.

The following table lists the location and color of each Link Speed LED on the Atlas3 B0 host card:

LED ID	Location	Color
LED12	Golden finger	**Blue**
LED10	EXT MCIO first port	**Blue**
LED9	INT MCIO first port	**Blue**
LED11	PCIe Straddle port	**Blue**

Each LED blinks at a frequency proportional to the negotiated PCIe link speed:

PCIe Generation	Blink Rate
Gen1	0.25 Hz
Gen2	0.5 Hz
Gen3	1 Hz
Gen4	2 Hz
Gen5	4 Hz
Gen6	Solid (steady on)

Link Width LEDs

These red LEDs report lane-width negotiation between the host card and connected device:

- **All LEDs off** – Full link width successfully negotiated (x16 for the monitored port group).
- **Single LED on** – Link is operating at a reduced width (x8, x4, or x2), depending on configuration or device capability.

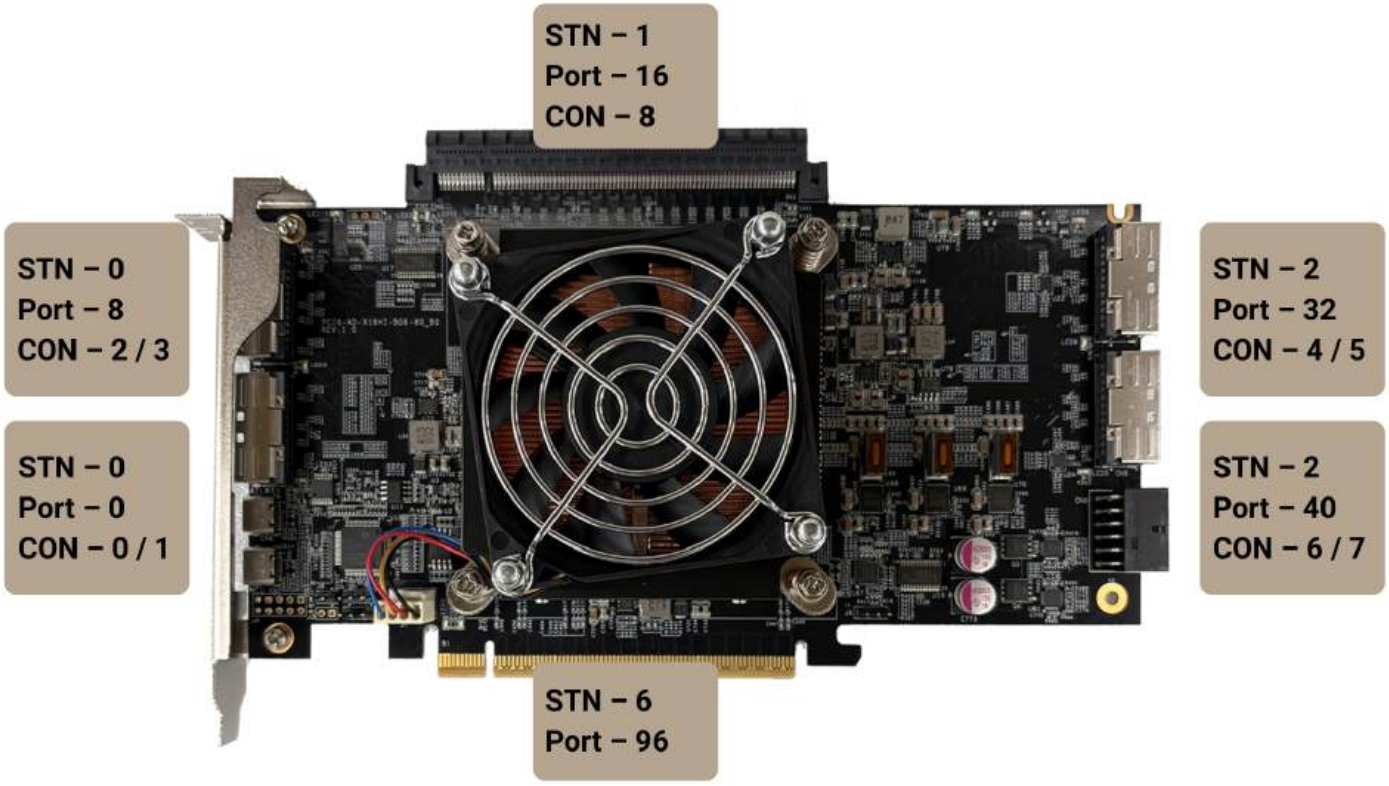
LED Pair	Monitored Port	All-Off Condition
LED1	Golden finger edge connector	Negotiated link width is x16/
LED3 / LED4	External MCIO ports	Negotiated link width is 1×16, 2×8, 4×4, or 8×2.
LED5 / LED6	Internal MCIO ports	Negotiated link width is 1×16, 2×8, 4×4, or 8×2.
LED 2	PCIe Straddle connector	Negotiated link width is x16.

For example, the EXT MCIO ports support x8×2 Dynamic Port Reconfiguration (DPR), allowing the x16 lane group to be split across multiple devices.

- When both EXT MCIO connectors operate as a full x16 group (e.g., 1×16, 2×8, 4×4, or 8×2), LED3 and LED4 are off, indicating full-width operation.
- When the upper and lower EXT MCIO connectors (e.g., CN4 / CN2) operate at reduced widths (such as 1×8, 2×4, or 4×2), one LED in the pair turns on, indicating reduced link width.

Port and Station Mapping

The Broadcom Atlas3 PEX90080 switch on the B0 host adapter includes five x16 stations. Each station maps to a specific group of PCIe lanes and connectors on the board.



The table below lists the lane allocation used on this card:

Station ID	Port Numbers	Connector Association
STN0	0, 8	External MCIO ports (CN2, CN4)
STN1	16	Golden finger edge connector
STN2	32, 40	Internal MCIO ports (CN3, CN5)
STN3	48 – 63	Reserved
STN6	96	PCIe Straddle connector (CN1)

Dynamic Port Reconfiguration (DPR) can re-map lane widths at runtime without reset, allowing bifurcation from x16 to x8 or x4 segments per use case. See **Port Link Status – showport** for more information on DPR.

CON Mapping for CLI Reference

Several CLI commands (e.g., **conrst**, **iicwr**, **iicw**) use logical CON numbers to address MCIO ports. The following mapping applies:

CON ID	Physical Connector	Port Number	I²C Channel	Associated Station
CON0/1	CN2	0	Channel A/B	STN0
CON2/3	CN4	8	Channel A/B	STN0
CON4/5	CN3	32	Channel A/B	STN2
CON6/7	CN5	40	Channel A/B	STN2
CON8	Golden finger edge connector	16	N/A	STN1

For example, **conrst 1** resets devices on CN2, while **iicwr d4 1 8 00** performs a write-then-read operation on device 0xD4 through CON0 Channel A, reading 8 bytes from register 0x00.

For more detail on these commands, please see **Command Usage Notes**.

Practical Applications and System Integration

The Atlas3 Host Adapter Card provides a flexible Gen6 platform for testing, validation, and deployment of PCIe 6.0 devices. It acts as a bridge between the host system and downstream hardware such as JBOFs, add-in cards, or SSD enclosures.

Built around Broadcom's Atlas3 PEX90144 switch, the card delivers high-speed fanout with very low latency. It's designed to handle demanding enterprise and engineering workloads where reliable, high-bandwidth PCIe connectivity is critical.

Connecting Gen6 JBOF Systems

The card is designed to interface directly with Serial Cables' **Gen6 8-Bay Passive JBOF** (Model: PCI6-ENC8-E3-08) using **MCIO6-8X-2X8B Y-cables**.

Each host card can access up to **eight x4 E3 or E1.S NVMe SSDs** when connected to a single JBOF chassis. In this configuration, the Atlas3 provides lane aggregation and switch management, while the JBOF functions as a transparent storage expansion enclosure.

Component	Description
Host Adapter	Atlas3 B0 Host Adapter (this product)
Cabling	MCIO6-8X-2X8B Y-cables (two required)
Target Device	Gen6 8-Bay Passive JBOF (PCI6-ENC8-E3-08)
Drive Support	Up to 8 × single-port x4 E3 / E1.S NVMe SSDs

Gen6 PCIe 8 bay E3 passive JBOF
[PCI5-ENC8-E3-08]

Direct-Attach SSD Testing

When connected with **MCIO x8 to dual-EDSFF (SFF-TA-1009)** cables, the host adapter can directly power and enumerate EDSFF drives for bench testing.

This setup supports single- or dual-port operation for **E1.S, E1.L, E2, or E3 NVMe SSDs**. It's commonly used for signal-integrity validation, firmware qualification, and drive interoperability testing.

Typical setup:

- One MCIO x8 port connects to two EDSFF drives through a dual-EDSFF interposer cable.
- Each MCIO port supports x8 total bandwidth, typically split into 2 × x4 links.
- Power, PERST#, and management signals are routed through the MCIO interface, with device status accessible via the switch.

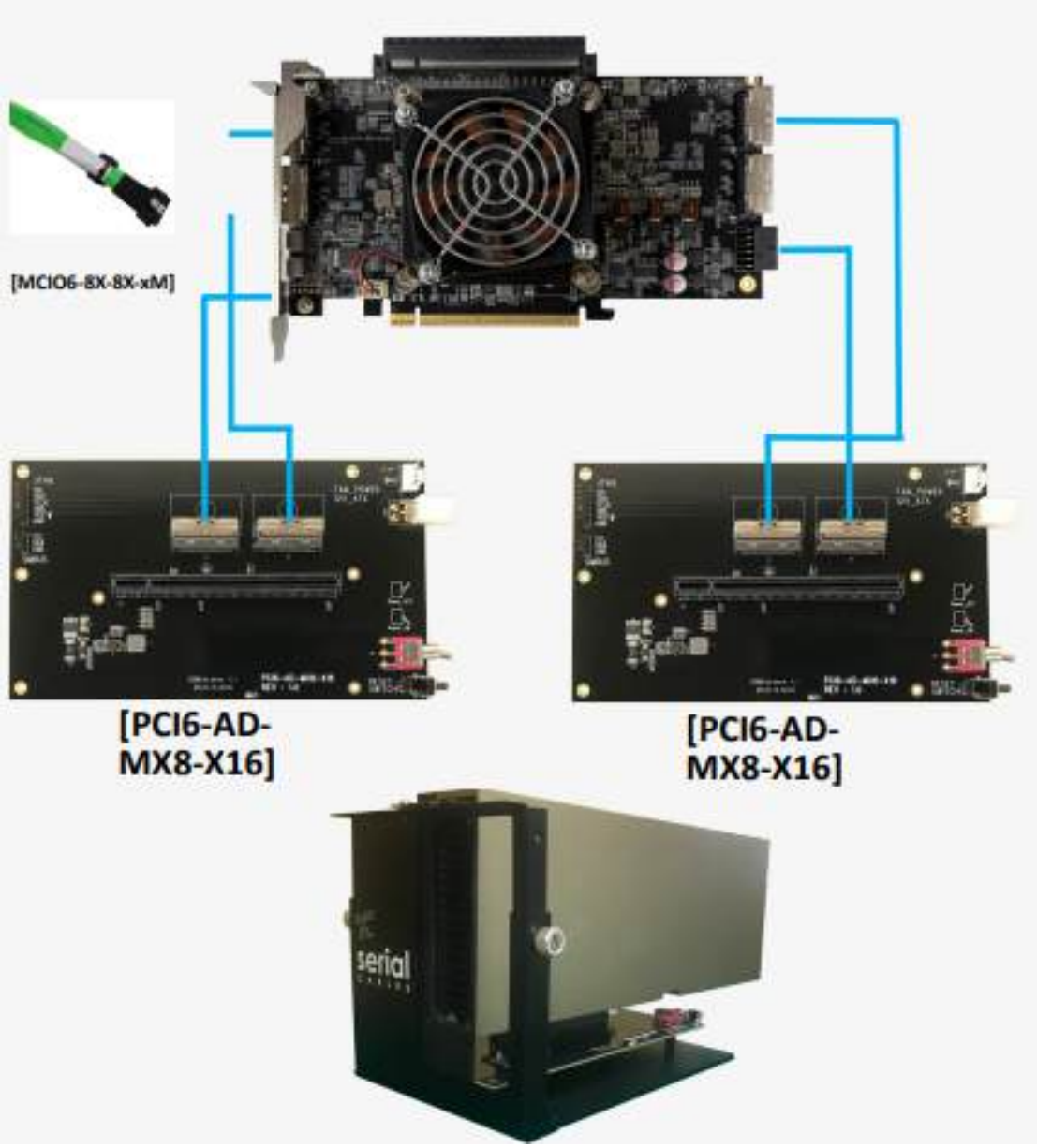
PCIe Slot Expansion

The Atlas3 B0 host adapter supports PCIe slot expansion using **MCIO6-8X-8X-xM cables** connected to the **PCI6-AD-MX8-X16** expansion board. This configuration enables additional PCIe Gen6 slots for add-in card testing and system expansion.

Each expansion board provides **two PCIe Gen6 x8 slots**, allowing connection of devices such as GPUs, NICs, accelerators, or storage HBAs.

Typical Setup:

- One MCIO x8 port connects to a PCI6-AD-MX8-X16 expansion board
- Each expansion board provides 2 × x8 PCIe slots
- Multiple MCIO ports can be used to connect additional expansion boards



Command-Line Interface (CLI) Setup

The Atlas3 B0 host adapter includes an onboard microcontroller (MCU) that provides configuration and diagnostic access to the Atlas3 switch. The MCU communicates through USB Type-C interfaces and exposes serial access for CLI and debug functions.

- **CN7 — Primary interface for CLI control**
- **CN6 — Secondary interface for SDB or SMART UART access (mode-dependent)**

All commands are executed directly on the MCU and do not require host drivers or software installation.

The CLI can be used to:

- Configure switch topology, port modes, and bifurcation.
- Monitor temperature, voltage, and link status.
- Access I²C devices on MCIO connectors.
- Perform firmware updates and diagnostics.

Connection Steps

1. Connect a USB Type-C cable between the host computer and the CN7 connector on the Atlas3 B0 card. (CN6 is not used for CLI commands.)

2. Power on the host system and confirm that the LED14 (heartbeat) and LED15 (MCU status) are both blinking.

3. Open your serial terminal software (Tera Term, PuTTY, or equivalent) and connect to the assigned COM port.

CLI Command Reference

Commands	Description
help	Display all available commands
fdl	Show MCU and Atlas3 switch firmware versions
lsd	Displays system telemetry, including temperature, critical voltages, fan speeds, and board power consumption
mw	Writes a 32-bit value to a specified register within the Atlas3 switch
dr	Dumps all switch-level registers for diagnostic or debugging purposes
dp	Dumps port-specific switch registers for the selected port
df	Dumps contents of the switch's onboard flash memory
conrst	Sends a PERST# signal (PCIe reset) with a 300ms pulse to devices attached via MCIO ports
showport	Displays link status and connection details for USP/DSP ports
bist	Runs the onboard Built-In Self-Test (BIST) for device diagnostics
setmode	Displays the current operational mode of the host card
spread	Configures the PCIe clock spread spectrum setting
clk	Enables or disables the PCIe clock output
sdb	Enables or disables Atlas3 SDB mode for external debug access
uart	Selects the CN6 UART path between SMART UART and the Atlas3 SDB interface
pwr	Displays power rail status, power-good signals, and overall board power sequence state
counters	Displays error counters and statistics for all active ports
flit	Configures FLIT (Flow Control Unit) disable mode
iicwr	Performs an SMBus "write-then-read" transaction to retrieve data from a device on an MCIO connector
iicw	Writes SMBus data to a device attached to an MCIO connector
ver	Displays version information for the host card, MCU firmware, and Atlas3 firmware
sysinfo	Shows general host card details and system information
reset	Performs a soft reset of the onboard MCU

Command Usage Notes

Firmware Upgrade and Management – fdl

The **fdl** command is used to upgrade the Atlas3 firmware, including unmanaged switch firmware, managed firmware, and MCU firmware. Firmware is transferred over the serial interface using the XMODEM protocol.

Enter the command **fdl** followed by the target upgrade mode. There are four to choose from:

- **mini** – Updates the unmanaged mini SBR firmware.
- **main** – Updates the unmanaged main SBR firmware.
- **fw** – Updates the managed switch firmware.
- **mcu** – Updates the on-board MCU firmware.

When executed, the system prompts for confirmation before erasing and writing flash memory.
Press **Y** to continue or **Ctrl+X** to cancel.

The **`mini`**, **`main`**, and **`fw`** commands erase and rewrite the corresponding switch flash regions.
Firmware data is transferred using the XMODEM protocol from the host system.

Firmware Upload Procedure

Step 1 – Connect via Serial Interface

- Connect a USB-C cable to the host card's CN7 port.
- Identify the COM port in your system's **Device Manager**.
- Open a terminal emulator such as **TeraTerm/puTTy** (Windows) or **minicom** (Linux) and connect to that COM port.
- A successful connection will display the command prompt (Cmd>).

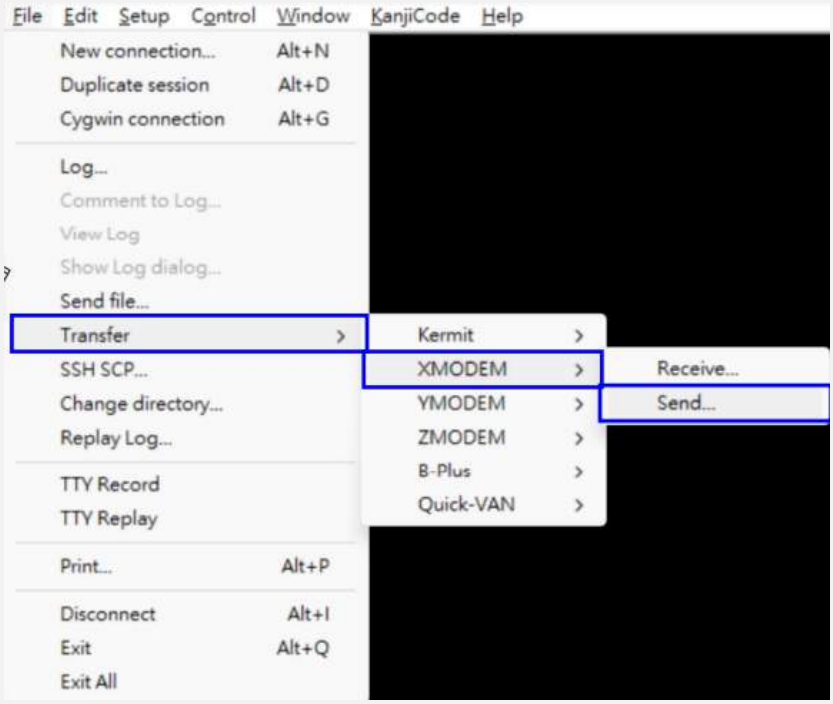
Step 2 – Run the Upload Command

1. Enter the appropriate **fdl** command (e.g., **fdl main**).
2. When prompted, press **Y** to confirm the upgrade or **Ctrl+X** to cancel.
3. The flash memory will be erased, and the system will wait for incoming data via XMODEM.

Continued on the next page.

Step 3 – Send the Firmware File via XMODEM

- In **TeraTerm** – Go to **File** → **Transfer** → **XMODEM** → **Send**, then select the **BIN firmware file**.



- In **minicom** – Use **Send File** → **XMODEM** and choose the **BIN firmware file**.

Step 4 – Apply the New Firmware

- After the upload finishes, power cycle the host card for unmanaged or managed firmware updates. For MCU firmware upgrades, use the **reset** command instead of a power cycle to activate the new MCU firmware.

System Diagnostics (Sensors and Power) – lsd

The **lsd** command displays real-time system diagnostics for the Atlas3 B0 host card, including temperature, fan speed, voltage readings, and power consumption. This information helps monitor board health, identify abnormal conditions, and verify proper cooling and power delivery.

The output includes:

- **Thermal** – Reports the temperature near the Atlas3 PCIe switch.
- **Fan Speed** – Shows the host card blower RPM.
- **Voltage Sensors** – Lists monitored onboard voltages.
- **Power Consumption** – Displays input voltage, current draw, and total board power in watts.

Register Write – mw

The **mw** command writes a 32-bit value to a specific register address within the Atlas3 PCIe switch. It writes the specified hexadecimal data directly to the target register, allowing configuration changes without requiring a reboot or reinitialization.

Enter the command **mw** followed by the register address (hex) and the data value (hex) to be written. Valid register addresses range from **0x00000000** to **0xFFFFFFFC**, and writable data values range from **0x00000000** to **0xFFFFFFFF**. For example:

- **mw fff0017c ffffffff** – This writes the data **0xFFFFFFFF** to the register address **0xFFF0017C** on the Atlas3 switch

Switch Register Dump – dr

The **dr** command reads and dumps switch-wide register values from the Atlas3 PCIe switch.
It retrieves low-level register data across the switch's address space for debugging, validation, and hardware bring-up.

Enter the command **dr** followed by the starting register address (hex) and an optional count (hex) to specify how many bytes to read. The valid register address range is **0x00000000** to **0xFFFFFFFC**. For example:

- **dr 60800000** – Dumps the values in Atlas3 switch registers starting from address 0x6080_0000.

Register Address Mapping

Each port's register block is mapped sequentially in memory, with offsets increasing by 0x8000 for each subsequent port. The table below lists the base address for key Atlas3 B0 port groups:

Port Type	Description	Base Address
EXT MICO	0	0x60800000
PCIe Straddle	16	0x60880000
INT MICO	32	0x60900000
Golden Finger	96	0x60B00000

Port Register Dump – dp

The **dp** command reads and dumps port-specific register values from the Atlas3 PCIe switch.
It displays low-level hardware data for a selected port, including configuration, link state, negotiated width, speed, and error counters. This command is mainly used to debug PCIe activity, check link training, or verify switch configuration.

Enter the command **dp** followed by the port number (0–111) to dump switch registers for that port. For example:

- **dp 32** – Dumps switch register values for Port 32.

Refer to CON Mapping for CLI Reference for more information.

Flash Dump — df

The **df** command reads and dumps the contents of the switch flash memory to the console or a connected host interface. It retrieves raw data from the onboard flash used for firmware storage and configuration retention, allowing engineers to inspect firmware images, configuration data, and diagnostics during development, debugging, or post-update verification.

Enter the command **df** followed by the start address (hex) and optionally the byte count (hex) to dump data from the switch flash memory. Both the address and count can range from 0x00000000 to 0xFFFFFFFC. For example:

- **df 400** – Dumps the contents of the Atlas3 flash starting from address 0x00000400
- **df 0 1000** – Dumps 4 bytes of flash data starting from address 0x00000400.

PCIe Reset to Attached Devices — conrst

The **conrst** command issues a PERST# (PCIe Reset) signal to devices connected through MCIO ports.
It issues a 300 ms reset pulse to either a specific station or all connectors, reinitializing attached devices such as SSDs, adapters, or other PCIe peripherals.

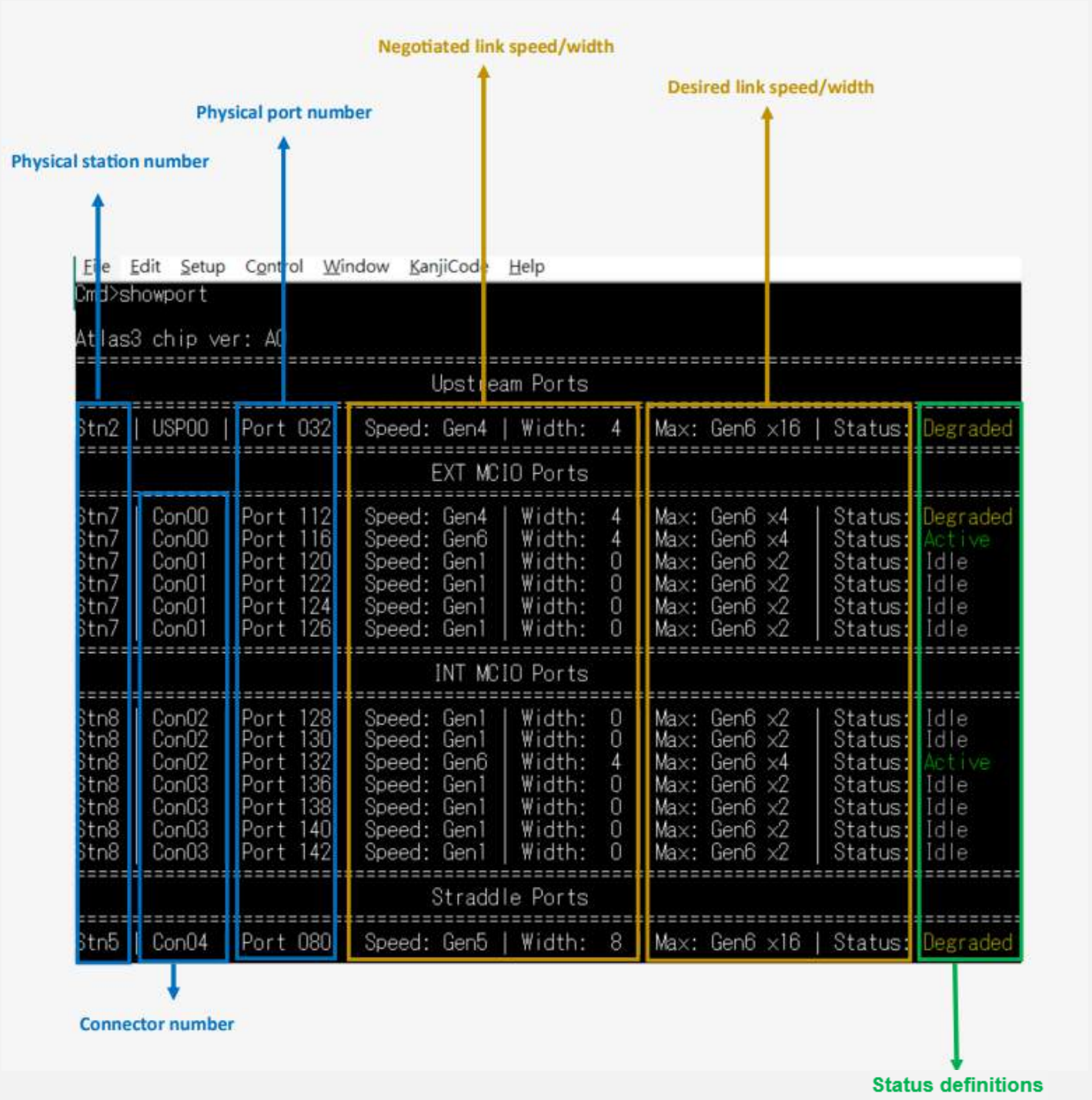
This process clears link and configuration errors without rebooting the system or reinitializing the switch, and is commonly used after hot-swapping or Dynamic Port Reconfiguration (DPR).

Enter the command **conrst** followed by the connector number (0–4) or **all**, and optionally specify the channel (**a** or **b**) to reset the corresponding MCIO device. For example:

- **conrst 1** – Sends a reset to the MCIO connector mapped to CON1.
- **conrst all** – Sends a reset to all MCIO connectors and the PCIe straddle port.

Port Link Status— showport

The **showport** command displays the link status for all upstream (USP) and downstream (DSP) ports on the Atlas3 PCIe switch. It retrieves and lists the link configuration for each port group, including **Upstream**, **EXT MCIO**, **INT MCIO**, and **Straddle Ports**. The output shows each port's station number, connector number, PCIe generation, negotiated width, maximum supported width, and current link status:



Output Field Descriptions

Field	Description
Station Number (Stn)	Physical station index on the host card.
Connector Number (Con)	Identifies the external or internal connector for the port.
Physical Port Number (Port)	Actual hardware port number assigned by the switch.
Speed	The **negotiated PCIe generation** (e.g., Gen1, Gen4, Gen6).
Width	The **negotiated link width** (e.g., x1, x4, x8, x16).
Max	The **maximum supported link** speed and width for the port.
Status	Current link condition (Active, Idle, or Degraded).

Status Definitions

- **Degraded** – Link trained successfully but negotiated speed or width is lower than expected.
- **Idle** – No physical link detected or device not present on the port.
- **Active** – Desired and negotiated link speed/width matched successfully.

Dynamic Port Reconfiguration (DPR)

Dynamic Port Reconfiguration (DPR) allows the Atlas3 PCIe switch to dynamically reassign, split, or merge lanes between ports without requiring a system reset. This feature enables operations such as **port bifurcation** (splitting lanes into smaller groups) or **port consolidation** (combining lanes) with minimal system impact.

The PCIe physical layer automatically updates link properties, such as width, polarity, and lane reversal, while maintaining active links on unaffected ports.

- DPR is implemented on both EXT MCIO and INT MCIO ports of the host adapter card.
- Each station contains x8 MCIO connectors for upper and lower EXT/INT ports, providing a total of x16 lanes per station.
- DPR can split a full x16 link into two x8 links or reassign groups of lanes to match the devices connected.

For example, connecting a Gen4 x4 device and a Gen6 x4 device within the same EXT MCIO group may consume available lanes and disable certain downstream x2 ports, depending on the configuration.

Built-In Self-Test — bist

The **bist** command runs a basic diagnostic routine on the Atlas3 host card. This function verifies overall hardware operation and checks communication between the MCU, PCIe switch, and all onboard I²C devices. It confirms that each connected I²C component, such as current shunt monitors, EEPROM, I/O expanders, I²C multiplexers, hot-swap controllers, and clock buffers, is responding correctly.

The test runs automatically once invoked and reports **OK** or **FAIL** results for each test item:

Channel	Device	Address	Status
CH0	PCA9575-0	0x40	OK
CH0	PCA9575-1	0x42	OK
CH1	PCA9575-2	0x44	OK
CH1	MP2971	0xBE	Fail
CH3	AT24C64	0xAE	OK

Host Card Mode Configuration — setmode

The **setmode** command sets the operating mode of the Atlas3 B0 host card. Each mode determines how the PCIe switch and ports are mapped, which connectors are active, and how the host card communicates with attached devices. Four default **SBR configuration files** are preloaded on the host card.

Enter the command **setmode** followed by the mode number (1–4) to configure the host card's operating mode.

Mode	Description
1	Host to switch golden finger port in **Common clock**. Precoding is **enabled**.
2	Host to switch golden finger port in **Common clock**. Precoding is **disabled**.
3	Host to switch golden finger port in **SRNS**. Precoding is **enabled**.
4	Host to switch golden finger port in **SRNS**. Precoding is **disabled**.

Precoding Behavior by Mode

- When precoding is **enabled** (Modes 1 and 3), the LTSSM automatically issues a transmitter precoding request during the EQ TS2 stage of PCIe link training.
    - The request updates the **Precoding Speed Select (12)** field in the **REC.RCVR.CFG** register for the active port.
    - The update is applied only when the **Write Enable** bit is set, ensuring the correct precoding value is programmed based on port and speed.
- When precoding is **disabled** (Modes 2 and 4), the LTSSM skips this step, allowing engineers to test raw, non-equalized link performance or validate baseline signal quality.

Show Host Card Mode — showmode

The **showmode** command displays the current operating mode of the Atlas3 B0 host card. Use it to confirm mode changes after running **setmode**.

PCIe Clock Spread Setting — spread

The **spread** command sets the fundamental PCIe reference clock to operate in CFC (Center Frequency Clocking) or SSC (Spread-Spectrum Clocking) mode. SSC uses **downspreading**, meaning the clock frequency periodically decreases from its nominal value (never above nominal), reducing EMI by distributing energy over a wider frequency band.

Enter the command **spread** followed by the **1**, **2**, or **off**:

Command	Downspread	Typical Use
spread 1	–3000 PPM (–0.3%)	When moderate EMI reduction is needed or devices are sensitive to timing variation.
spread 2	–5000 PPM (–0.5%)	When maximum EMI reduction or PCIe SSC compliance is required.
spread off	None	When performing precision timing, signal integrity, or jitter testing.

PCIe Clock Output Control – clk

The **clk** command controls the PCIe clock output signal from the Atlas3 B0 host card. It enables or disables the clock output to downstream or attached devices through the PCIe straddle connector, EXT MCIO connectors, and INT MCIO connectors. This command is primarily used during system bring-up, link debugging, or when verifying signal presence to attached peripherals.

- **clk en** – Enable PCIe clock output
- **clk dis** – Disable PCIe clock output

Clock Output Guidelines

- Clock output can be changed dynamically and does not require a host card power cycle.
- The setting is stored in the MCU and applied automatically the next time the host card powers on.
- Disabling clock output prevents attached devices from receiving the PCIe reference clock needed for link training.

SDB Port Control — sdb

The **sdb** command enables or disables the Atlas3 Serial Debug Bridge (SDB) interface. This controls whether the board operates in normal MCU-driven CLI mode or exposes the SDB interface for external debug utilities.

Enter the command **sdb** followed by **off** or **on**:

Command	Description	Typical Use
sdb off	Disables SDB mode.	Used for **normal operation** like running CLI commands such as **fdl**, **mw**, **dr**, **dp**, and **showport.**
sdb on	Enables SDB mode.	Used for **utility mode** – running host-based tools such as **SwitchCLID** or **ARCTIC** from a PC.

SDB Behavior Notes

- Only one mode is active at a time (MCU CLI or SDB utilities).
- Enabling SDB mode redirects control away from normal CLI operation.
- The selected mode remains active until changed or the board is reset.

Utilities such as SwitchCLID and ARCTIC are Broadcom-provided tools distributed under NDA and SLA. Contact Broadcom for licensing, access, or additional support information.

UART Path Selection — uart

The **uart** command selects the UART path for the CN6 (USB Type-C) interface, switching between the Atlas3 SDB (Serial Debug) interface and the SMART UART interface.

Enter the command **uart** followed by **0** or **1**:

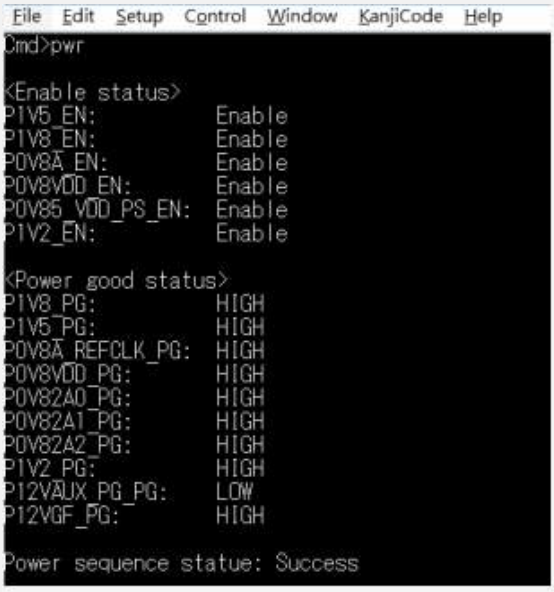
- **uart 0** – Route CN6 to SMART UART
- **uart 1** – Route CN6 to SDB (default)

UART Path Notes

- The selected UART path is stored and applied after a power cycle.
- SDB (Serial Debug) is supported in both managed and unmanaged firmware modes.
- SMART UART is supported only in managed firmware mode.

Power Status — pwr

The **pwr** command displays the current power status of the Atlas3 B0 host adapter, including power rail enable states, power-good signals, and overall power sequencing status. A “Success” power sequence status indicates all required rails initialized correctly



Port Error Counters — counters

The **counters** command displays accumulated error counts and status information for all active ports on the Atlas3 PCIe switch. These counters track transmission and protocol-level faults such as bad TLPs, DLLPs, or link drops. Use this command to monitor link stability and detect potential hardware or signal integrity issues.

- **counters** – Displays the current error counts for all ports.
- **counters clear** – Resets all port error counters to zero.

About Error Counter Behavior

- Each counter increments by 1 when an error event is detected, as defined in the FLIT Error Counter Control Register.
- When enabled, counters decrement automatically at a fixed rate if non-zero, depending on encoding and link width.
- All counters are cleared when:
  - **counters clear** is executed
  - The switch or MCU resets
  - The FLIT Error Counter Enable bit transitions from **0b** to **1b**

FLIT Mode Control — flit

The `flit` command controls FLIT disable mode on Atlas3 PCIe ports. FLIT (Flow Control Unit) mode is used in PCIe Gen5 and Gen6 to segment and transmit data efficiently.

Enter **flit** followed by either **all** or a station ID (0, 1, 2, or 6), then specify **on** or **off**. Enter **flit** by itself to view which stations are enabled and which are disabled. For example:

- **flit 2 off** – Disables FLIT disable mode on station 2
- **flit all on** – Enables FLIT disable mode (default for Gen 5 and later) on all stations

Station IDs follow the host card station mapping defined in Port and Station Mapping. For B0, valid station IDs are 0, 1, 2, and 6.

About FLIT Disable Mode

- nabling FLIT disable mode prevents the port from advertising FLIT support during link training.
- This setting does not modify the FLIT capability reported in PCIe configuration registers.
- FLIT mode is required for operation at 64 GT/s (Gen6). Disabling FLIT will prevent links from training at Gen6 speeds.

SMBus Read (write-then-read) — iicwr

The `iicwr` command performs a write-then-read SMBus transaction to devices attached through the MCIO connectors. It first writes a register offset, then reads data back from the same device.

The MCU acts as the SMBus master and communicates with devices through the MCIO sideband interface. Each MCIO connector provides two SMBus channels (A and B):

- **Channel A** — pins B8/B9
- **Channel B** — pins B26/B27

Enter **iicwr** followed by the device address (hex), CON ID (0–7), MCIO channel (a or b), read length (1–128 bytes), and the write data byte (hex). For example:

- **iicwr d4 0 a 8 0** – Read 8 bytes starting at register 0x00 from device 0xD4 on CON0, channel a

CON ID corresponds to the logical connector index. See CON Mapping for CLI Reference.

SMBus Write — iicw

Writes SMBus data to devices attached to MCIO connectors. Commonly used to configure EEPROMs, sensors, or retimers.

Enter the command **iicw** followed by the device address (hex), CON ID (0–8), MCIO channel (a or b), and one or more data bytes (hex) to write. For example:

- **iicw d4 0a ff** – Write 0xFF to device 0xD4 on CON0, channel a

System Version — ver

Shows current firmware versions for both the MCU and the Atlas3 switch. Use this command to verify the running build before or after a firmware update.

---------- Product Info ----------	
Company :	Serial Cables
Model :	PCI6-AD-x16HI-BG6-80-B0
Serial No. :	
---------- App Info ----------	
Version :	0.0.2
Build Time :	Apr 17 2026 03:03:36
---------- SBR Info ----------	
Version:	0022B004
Switch Mode:	Unmanaged mode

System Information — sysinfo

Displays a complete summary of the hardware identity and power source data for the Atlas3 host adapter, including board ID, serial number, and switch details.

This is effectively a sequence of several key commands (**ver**, **lsd**, **clk**, **showport**, **bist**), consolidated into a single report for quick system validation.

System Reset — reset

Performs a soft reset of the MCU and Atlas3 switch. This clears all volatile configuration registers, retrains PCIe links, and reinitializes switch management logic.

Enter the command **reset** followed by an optional reset type to control how the host card is reset. For example:

- **reset** – Reset the onboard MCU and power cycle the host adapter.
- **reset s0** – Issue a PERST# reset to the PCIe hierarchy (reset attached devices and retrain links without power cycling the board).
- **reset sw** – Issue a system power-on reset to reinitialize the PCIe switch and system logic.

Maintenance & Diagnostics

The Atlas3 B0 Host Adapter Card includes built-in utilities for monitoring system health and diagnosing link, power, or temperature-related issues. Performing regular checks helps maintain stable operation and identify faults early.

- Run **lsd** to confirm all fans are spinning and temperature sensors are reading normally.
- Use **sysinfo** before and after maintenance to log current firmware, power, and system status.
- After connecting or reseating downstream devices, run **showport** to confirm all ports are trained and operating at the expected link width and speed.
- If **LED13 remains illuminated**, it may indicate a thermal fault, power anomaly, or failed link. Run **bist** or review system telemetry via **lsd** for diagnostics.

Revision History

Revision	Description
1.1	Reformatted and restyled for brand consistency and readability. Rewritten for clarity. Added *Product Overview*, *Safety, Handling & Compliance*, *Maintenance & Diagnostics,* and *Contact Us* sections.
1.0	Initial manual release.

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