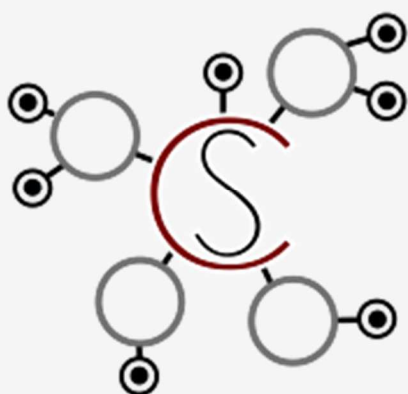




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PCIe/CXL Gen5 Vertical Type MCIO Retimer Based Host Card

User's Manual

REV: 1.1

July. 2025

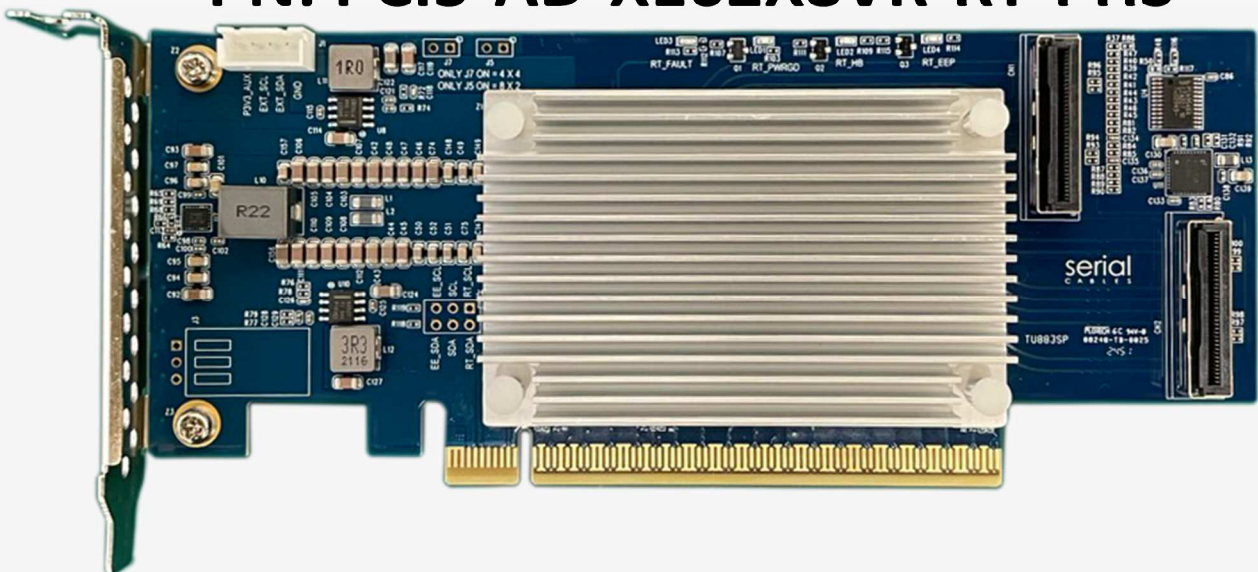


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PN: PCI5-AD-X162X8VR-RT

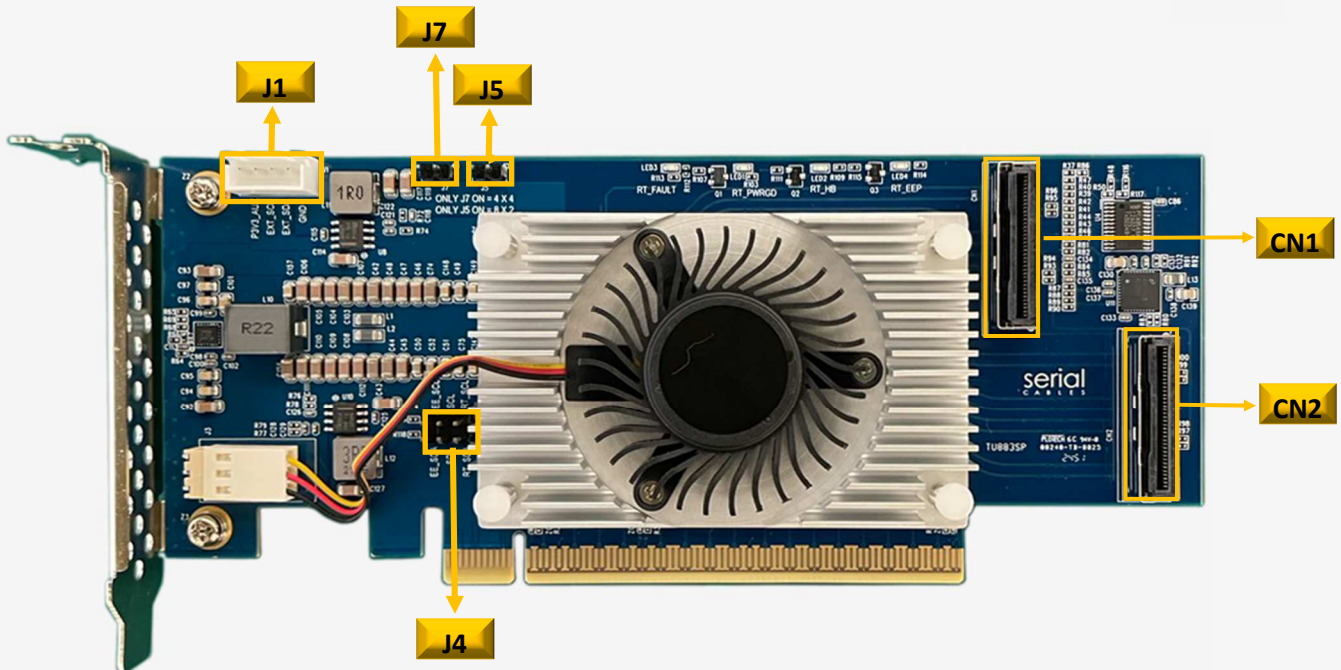


PN: PCI5-AD-X162X8VR-RT-PHS





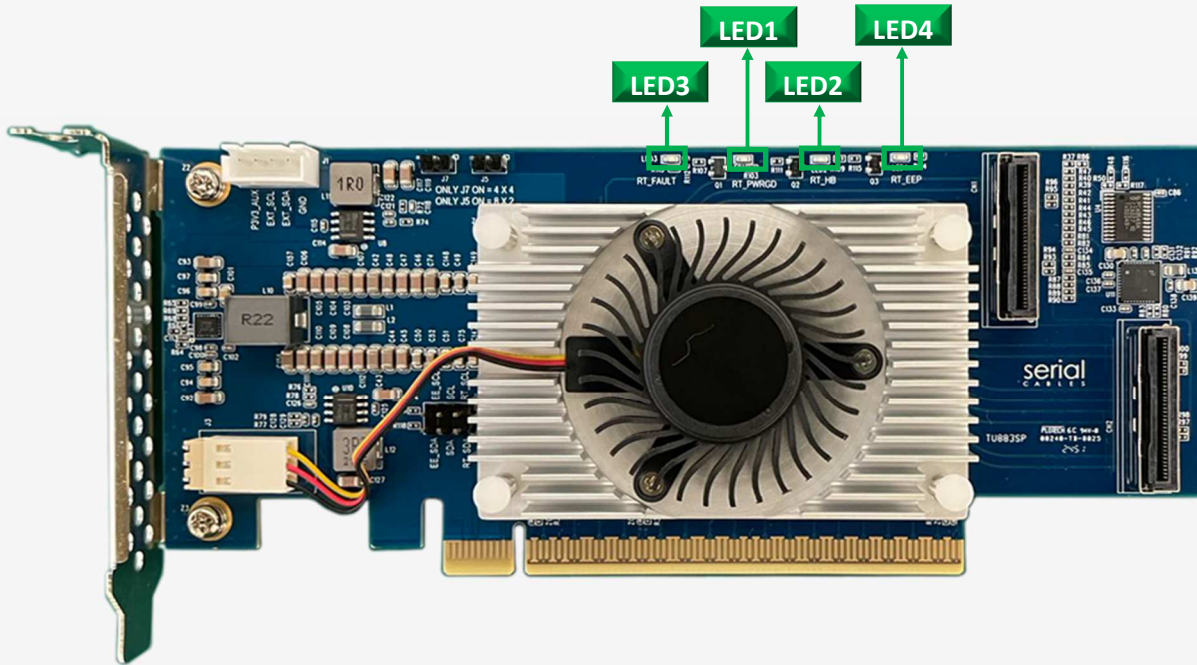
Function Description For Headers And Connectors



Headers	Descriptions															
J5/J7	Have Jumper ON in J7 only=Retimer supports 4x4 bifurcations in two x8 MCIO connectors. J5 only= Retimer supports 8x2 bifurcations in two x8 MCIO connectors.															
J4	SMbus accessing selection. Pin 1&3_2&4 ON=To select the SMBus from J1 to connect to RETIMER IC(DEFAULT). Pin 3&5_4&6 ON=To select the SMBus from J1 to connect to EEPROM of RETIMER IC. <table border="1"><tr><td>Pins in Header</td><td>5</td><td>3</td><td>1</td></tr><tr><td rowspan="2">Signals</td><td>EE_SCL</td><td>SCL</td><td>RT_SCL</td></tr><tr><td>EE_SDA</td><td>SDA</td><td>RT_SDA</td></tr><tr><td>Pins in Header</td><td>6</td><td>4</td><td>2</td></tr></table>	Pins in Header	5	3	1	Signals	EE_SCL	SCL	RT_SCL	EE_SDA	SDA	RT_SDA	Pins in Header	6	4	2
Pins in Header	5	3	1													
Signals	EE_SCL	SCL	RT_SCL													
	EE_SDA	SDA	RT_SDA													
Pins in Header	6	4	2													
CN1/CN2	Vertical type MCIO x8 74Pins connectors															
J1	External SMBus Interface <table border="1"><tr><td>Signals</td><td>P3V3_AUX</td><td>EXT_SCL</td><td>EXT_SDA</td><td>GND</td></tr><tr><td>Pins in Header</td><td>1</td><td>2</td><td>3</td><td>4</td></tr></table>	Signals	P3V3_AUX	EXT_SCL	EXT_SDA	GND	Pins in Header	1	2	3	4					
Signals	P3V3_AUX	EXT_SCL	EXT_SDA	GND												
Pins in Header	1	2	3	4												



Function Description For LEDs



Location	Color	Description
LED3	Red	<u>Retimer fault LED</u> Lights if any error detected in retimer IC.
LED1	Blue	<u>Retimer card power good LED</u> Lights to indicate all of power rails in retimer host card output correctly.
LED2	Green	<u>Retimer card heartbeat LED</u> <u>Blinking as heartbeat for retimer FW.</u>
LED4	Blue	<u>Retimer EEPROM read done LED</u> Lights to indicate retimer IC reading FW from EEPROM completed and successfully.



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PCIe/CXL Retimer Host Card

MCIO Pin Definition



CN1		2	3	5	6	8	9
	A	A_PETN7	A_PETP7	A_PETN6	A_PETP6	MCIO_SCL_A0	MCIO_SDA_A0
	B	B_PERN7	B_PERP7	B_PERN6	B_PERP6	NC	NC
		14	15	17	18	11	12
	A	A_PETN5	A_PETP5	A_PETN4	A_PETP4	RT_PERST#	NC
	B	B_PERN5	B_PERP5	B_PERN4	B_PERP4	MCIO_CLKA_P0	MCIO_CLKA_N0
		20	21	23	24	26	27
	A	A_PETN3	A_PETP3	A_PETN2	A_PETP2	MCIO_SCL_B0	MCIO_SDA_B0
	B	B_PERN3	B_PERP3	B_PERN2	B_PERP2	NC	NC
		32	33	35	36	29	30
	A	A_PETN1	A_PETP1	A_PETN0	A_PETP0	RT_PERST#	NC
	B	B_PERN1	B_PERP1	B_PERN0	B_PERP0	MCIO_CLKB_P0	MCIO_CLKB_N0

CN2		2	3	5	6	8	9
	A	A_PETN15	A_PETP15	A_PETN14	A_PETP14	MCIO_SCL_A1	MCIO_SDA_A1
	B	B_PERN15	B_PERP15	B_PERN14	B_PERP14	NC	NC
		14	15	17	18	11	12
	A	A_PETN13	A_PETP13	A_PETN12	A_PETP12	RT_PERST#	NC
	B	B_PERN13	B_PERP13	B_PERN12	B_PERP12	MCIO_CLKA_P1	MCIO_CLKA_N1
		20	21	23	24	26	27
	A	A_PETN11	A_PETP11	A_PETN10	A_PETP10	MCIO_SCL_B1	MCIO_SDA_B1
	B	B_PERN11	B_PERP11	B_PERN10	B_PERP10	NC	NC
		32	33	35	36	29	30
	A	A_PETN9	A_PETP9	A_PETN8	A_PETP8	RT_PERST#	NC
	B	B_PERN9	B_PERP9	B_PERN8	B_PERP8	MCIO_CLKB_P1	MCIO_CLKB_N1

Note: It follows the pinout in MCIO as defined SFF9402, but reverse all signals between A and B side.