



PCIe/CXL Gen6 Retimer Card

PCI6-AD-2xMCIO-2xMCIO-RT-BC

User's Manual

REV: 1.0

Jul. 2025

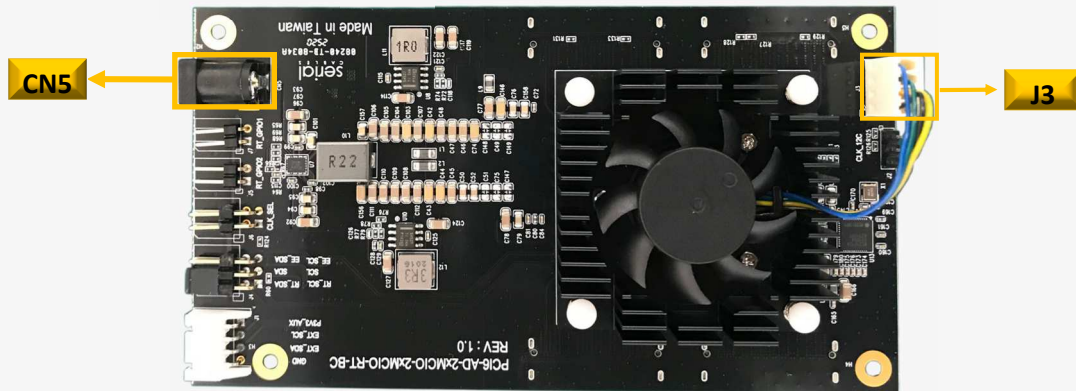


Dimensions	76 x 140 x 24mm (W*L*H) Height includes FAN-sink and MCIO connectors
Connectors	1x 12V DC JACK 4x MCIO SFF-TA-1016 connectors 1x 1R4P 2.54mm FAN connector
Redriver IC	Broadcom Gen6 Retimer BCM85667 Compatible with PCIe Gen6/Gen5/Gen4/Gen3/Gen2/Gen1 and Compute Express Link (CXL 3.1) standards Extends reach to >36 dB at 64 GT/s Supports parallel lane groupings per transfer: <u>One 16-lane link (1x 16)</u> <u>Two 8-lane links (2x 8)</u> <u>Four 4-lane links (4x 4)</u> <u>Eight 2-lane links (8x 2)</u>
Power	Maximum 10.2W, operated in Gen6 64-GT/s 1x 16.
Operating Temperature	0 C to +40 C
Storage Temperature	-40 C to 85 C
Operating Humidity	10% to 90% relative humidity non-condensing
Storage Humidity	5% to 95% relative humidity non-condensing
Drivers / Software	Requires no software / driver installation

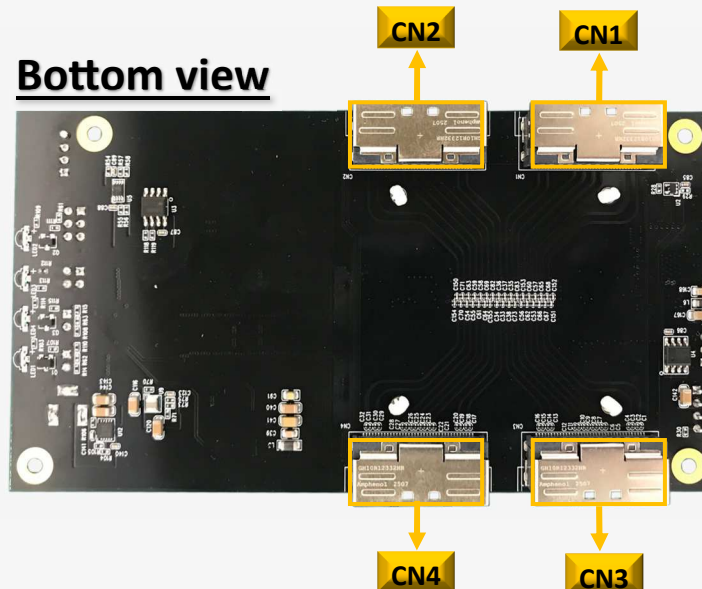


Functions Of Connectors

Top view



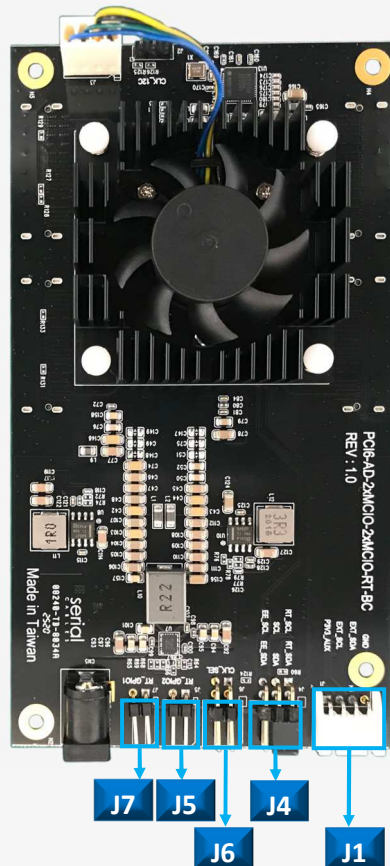
Bottom view



Location	Descriptions
CN1 CN2	MCIO X8 Connectors in SFF9402 Root pinout
CN3 CN4	MCIO X8 Connectors in SFF9402 Endpoint pinout
CN6	DC Jack for P12V AC adapter



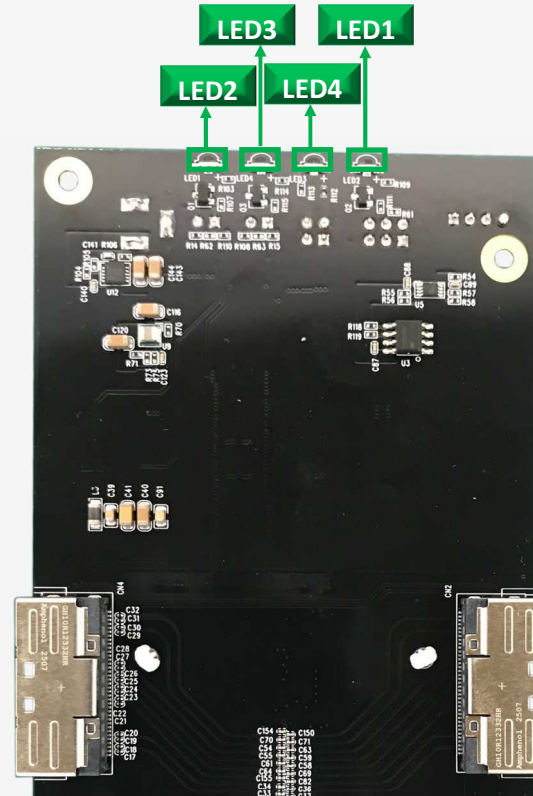
Functions Of Headers



Headers	Descriptions																		
J5/J7	Reserved for bifurcation selection																		
J4	SMBus accessing selection. Pin 1&3_2&4 ON=To select the SMBus from J1 to connect to RETIMER IC(DEFAULT). Pin 3&5_4&6 ON=To select the SMBus from J1 to connect to EEPROM of RETIMER IC. <table><tr><td>Pins in Header</td><td>5</td><td>3</td><td>1</td></tr><tr><td rowspan="2">Signals</td><td>EE_SCL</td><td>SCL</td><td>RT_SCL</td></tr><tr><td>EE_SDA</td><td>SDA</td><td>RT_SDA</td></tr><tr><td>Pins in Header</td><td>6</td><td>4</td><td>2</td></tr></table>				Pins in Header	5	3	1	Signals	EE_SCL	SCL	RT_SCL	EE_SDA	SDA	RT_SDA	Pins in Header	6	4	2
Pins in Header	5	3	1																
Signals	EE_SCL	SCL	RT_SCL																
	EE_SDA	SDA	RT_SDA																
Pins in Header	6	4	2																
J6	Reserved for Retimer clock mode selection																		
J1	External SMBus Interface <table><tr><td>Signals</td><td>P3V3_AUX</td><td>EXT_SCL</td><td>EXT_SDA</td><td>GND</td></tr><tr><td>Pins in Header</td><td>1</td><td>2</td><td>3</td><td>4</td></tr></table>				Signals	P3V3_AUX	EXT_SCL	EXT_SDA	GND	Pins in Header	1	2	3	4					
Signals	P3V3_AUX	EXT_SCL	EXT_SDA	GND															
Pins in Header	1	2	3	4															



Function Description For LEDs



Bottom view

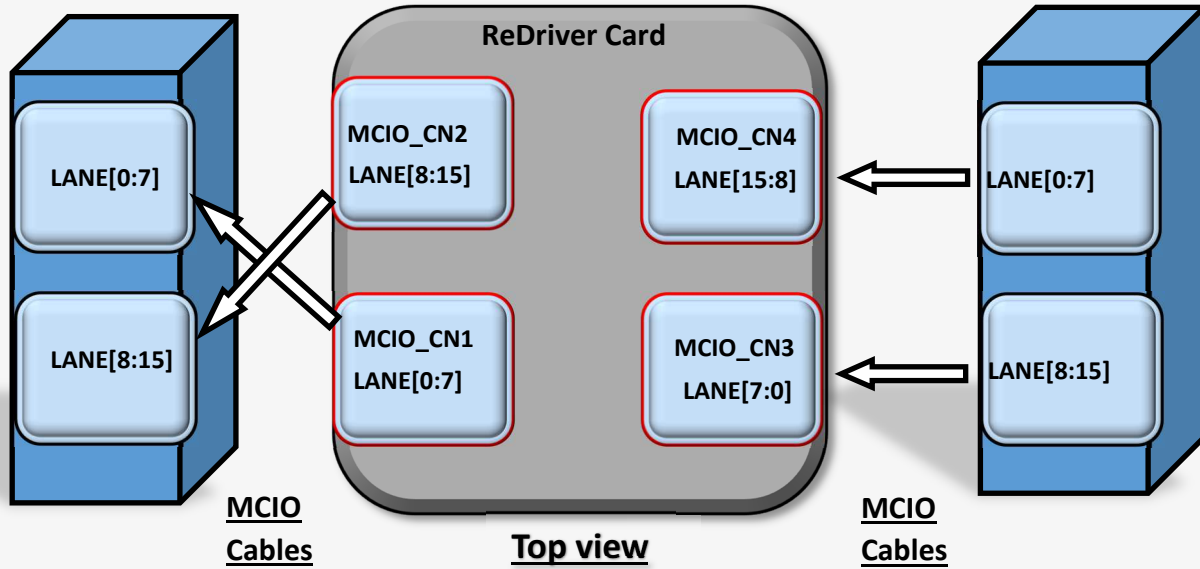
Location	Color	Description
LED1	Blue	<u>Retimer card power good LED</u> Lights to indicate all of power rails in retimer host card output correctly.
LED4	Blue	<u>Retimer EEPROM read done LED (reserved)</u> Lights to indicate reitmer IC reading FW from EEPROM completed and successfully.
LED3	Red	<u>Retimer fault LED (reserved)</u> Lights if any error detected in retimer IC.
LED2	Green	<u>Retimer card heartbeat LED (reserved)</u> <u>Blinking as heartbeat for retimer FW.</u>



Back Plane Board/

Endpoint

Root/Server



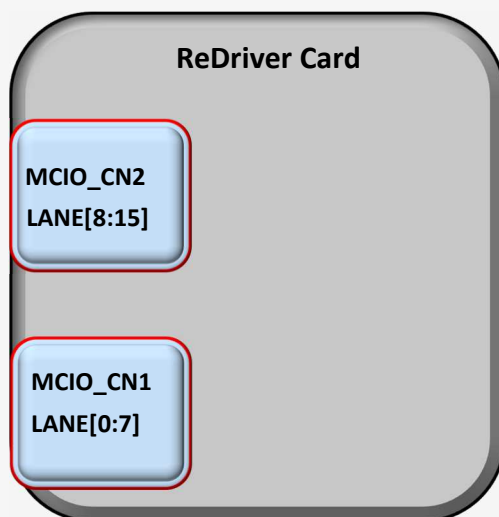
Above x16 links connection was based on “no lane reverse” in both of root and end-point devices.

Please always check the pinout of in both sides and have cables connection correctly in x16 links.



MCIO Pins Definition

Top View



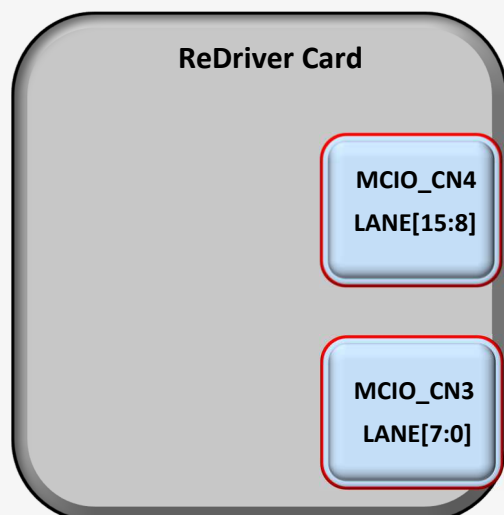
CN1	2		3		5		6		8		9	
	A	B_PERP0	B_PERN0	B_PERP1	B_PERN1	NC		NC				
	B	A_PETP0	A_PETN0	A_PETP1	A_PETN1	MCIO_HSCL_A0		MCIO_HSDA_A0				
	14		15		17		18		11		12	
	A	B_PERP2	B_PERN2	B_PERP3	B_PERN3	MCIO_CLKA_P0		MCIO_CLKA_N0				
	B	A_PETP2	A_PETN2	A_PETP3	A_PETN3	RT_PERST#		NC				
	20		21		23		24		26		27	
	A	B_PERP4	B_PERN4	B_PERP5	B_PERN5	NC		NC				
	B	A_PETP4	A_PETN4	A_PETP5	A_PETN5	MCIO_HSCL_B0		MCIO_HSDA_B0				
	32		33		35		36		29		30	
	A	B_PERP6	B_PERN6	B_PERP7	B_PERN7	MCIO_CLKB_P0		MCIO_CLKB_N0				
	B	A_PETP6	A_PETN6	A_PETP7	A_PETN7	RT_PERST#		NC				

CN2	2		3		5		6		8		9	
	A	B_PERP8	B_PERN8	B_PERP9	B_PERN9	NC		NC				
	B	A_PETP8	A_PETN8	A_PETP9	A_PETN9	MCIO_HSCL_A1		MCIO_HSDA_A1				
	14		15		17		18		11		12	
	A	B_PERP10	B_PERN10	B_PERP11	B_PERN11	MCIO_CLKA_P1		MCIO_CLKA_N1				
	B	A_PETP10	A_PETN10	A_PETP11	A_PETN11	RT_PERST#		NC				
	20		21		23		24		26		27	
	A	B_PERP12	B_PERN12	B_PERP13	B_PERN13	NC		NC				
	B	A_PETP12	A_PETN12	A_PETP13	A_PETN13	MCIO_HSCL_B1		MCIO_HSDA_B1				
	32		33		35		36		29		30	
	A	B_PERP14	B_PERN14	B_PERP15	B_PERN15	MCIO_CLKB_P1		MCIO_CLKB_N1				
	B	A_PETP14	A_PETN14	A_PETP15	A_PETN15	RT_PERST#		NC				



MCIO Pins Definition

Top View



CN3	2		3		5		6		8		9	
	A	A_PERN7	A_PERP7	A_PERN6	A_PERP6	MCIO_HSCL_A0		MCIO_HSDA_A0				
	B	B_PETN7	B_PETP7	B_PETN6	B_PETP6	NC		NC				
	14		15		17		18		11		12	
	A	A_PERN5	A_PERP5	A_PERN4	A_PERP4	RT_PERST#		MCIO_CRT#_IN_A0				
	B	B_PETN5	B_PETP5	B_PETN4	B_PETP4	MCIO_CLKOUTN_A0		MCIO_CLKOUTP_A0				
	20		21		23		24		26		27	
	A	A_PERN3	A_PERP3	A_PERN2	A_PERP2	MCIO_HSCL_B0		MCIO_HSDA_B0				
	B	B_PETN3	B_PETP3	B_PETN2	B_PETP2	NC		NC				
	32		33		35		36		29		30	
	A	A_PERN1	A_PERP1	A_PERN0	A_PERP0	NC		MCIO_CRT#_IN_B0				
	B	B_PETN1	B_PETP1	B_PETN0	B_PETP0	NC		NC				

CN4	2		3		5		6		8		9	
	A	A_PERN15	A_PERP15	A_PERN14	A_PERP14	MCIO_HSCL_A1		MCIO_HSDA_A1				
	B	B_PETN15	B_PETP15	B_PETN14	B_PETP14	NC		NC				
	14		15		17		18		11		12	
	A	A_PERN13	A_PERP13	A_PERN12	A_PERP12	NC		MCIO_CRT#_IN_A1				
	B	B_PETN13	B_PETP13	B_PETN12	B_PETP12	MCIO_CLKOUTN_A1		MCIO_CLKOUTP_A1				
	20		21		23		24		26		27	
	A	A_PERN11	A_PERP11	A_PERN10	A_PERP10	MCIO_HSCL_B1		MCIO_HSDA_B1				
	B	B_PETN11	B_PETP11	B_PETN10	B_PETP10	NC		NC				
	32		33		35		36		29		30	
	A	A_PERN9	A_PERP9	A_PERN8	A_PERP8	NC		MCIO_CRT#_IN_B1				
	B	B_PETN9	B_PETP9	B_PETN8	B_PETP8	NC		NC				