PCIe Gen5 E3.S To M.2 Adapter Card

PCI5-AD-E3M2-1X4

User's Manual

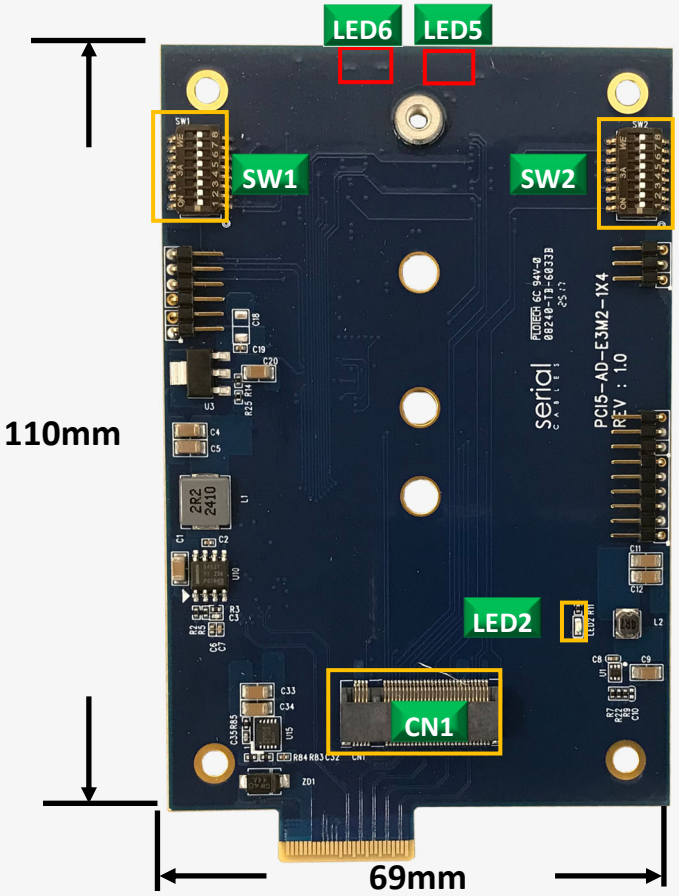
REV: 1.0

Jul. 2025

Change History

REV	Change history	Date of Release
1.0	New created	July. 2025

PCB Dimension And Connectors



Location	Descriptions
CN1	PCIe Gen5 M.2 Connectors. Height=3.2mm
LED2	Green M.2 Activity LEDs
LED5	Red Host LED. Controlled by EDSFF connector Pins_A11
LED6	Blue 3.3V Power LED.
SW1/SW2	Piano switch, refer to page 4 for more detail descriptions

Functions For Piano Switch

SW1		
Pins	Pins	Description
16	15	ON: connect M2_CLKREQ# to EDSFF_CLKREQ#
14	13	ON: Disable M.2 3.3V output
12	11	NC
10	9	ON: Set M.2_PWRDIS_0 to “H”
8	7	NC
6	5	ON: Set EDSFF_PERST#_0 to “H”
4	3	NC
2	1	ON: Set M.2_0 PERST# to “L”

SW2		
Pins	Pins	Description
16	15	ON: Set TMP112A_ADD0 to “L”
14	13	ON: Set EDSFF_PWRDIS to “H”
12	11	ON: Set EDSFF_SMDAT with 3.3V PU
10	9	ON: Set EDSFF_SMCLK with 3.3V PU
8	7	NC
6	5	ON: Set M.2_PRSNT# to “L”
4	3	NC
2	1	ON: Set M.2_VIO1V8 to P1V8

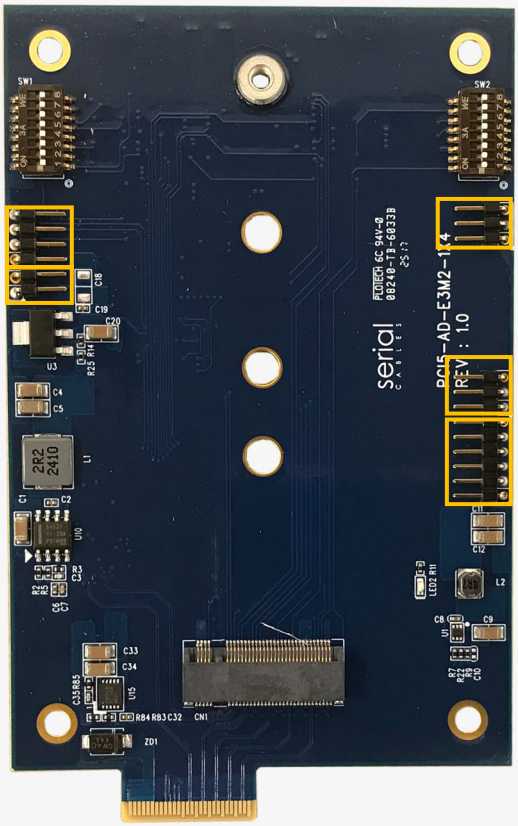
Functions For Headers

J6

Pins	Name
M.2_Pin40	M2_SMCLK_0
M.2_Pin42	M2_SMDAT_0
M.2_Pin44	M2_ALERT#_0
	GND

J11

Name
P1V8
M2_VIO
P3V3



J7

Pins	Name
	GND
M.2_Pin56	M2_MFG_DATA
M.2_Pin58	M2_MFG_CLOCK

J1

M.2 clock selection
OFF: M.2 works in SRNS mode
ON : M.2 works in CC mode

J2

Pins	Name
	GND
M.2_Pin8	M2_PLN#_0
M.2_Pin32	M2_PLA_S3#_0
M.2_Pin68	M2_SUSCLK_0
M.2_Pin73	M2_VIOCFG_0
M.2_Pin54	M2_PEWAKE#_0