PHISON PS7161
PCIE 6.0 REDRIVER IC
Preliminary DATASHEET

V1.1 Jun. 11, 2025

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REVISION HISTORY

Revision	Description	Draft Date
0.1	● Initial release	Sep. 27, 2024
0.2	● Adjust Table of contents, List of Tables, List of Figures	Sep. 30, 2024
0.3	● Adjust Table of PS7161/PS7162 I²C Slave ID Mapping for 2 Different Types	Oct. 23, 2024
0.4	● Add description in CHA8 **PCB AND STENCIL GUIDE**	Dec. 6, 2024
0.5	● Modify **Figure 3: Finite State Machine**, switch the location of RX +/- Inactive and Active	Jan. 6, 2025
0.6	● Modify **Figure 7: Power On Sequence for PS7161 I2C Mode** ● Modify 4.5.5 **Power-On Sequence**	Mar. 5, 2025
0.7	● Add Case Temperature of device in **1.2 Features** ● Add Case Temperature of device in **Table 5: The Recommended Operating Conditions** ● Add Chapter 7**: PS7161 Batch File Guides for VNA Test** ● Remove I_{ULPM} in **Table 6: DC Electrical Characteristic List**	Apr. 16, 2025
0.8	● Modify data in **3.1 Absolute Maximum Ratings**, **3.3 DC Electrical Characteristics**, and **3.4 High Speed Electrical Characteristics**. ● Modify data in **4.3.2 Linear Equalization**, **4.3.3 Driver Swing (16GHz)**	May. 6, 2025
0.9	● Update data in **Table 31: Thermal Resistance of PS7161**	May. 13, 2025
1.0	● Add **Chapter 4.5.6: The "Detect counter" feature of the Redriver RX detection function is enabled by default in compatibility test.**	Jun. 6, 2025
1.1	● **Modify Chapter 2.2: Pin Functions,** the description of PERST_N and CLKREQ_N in **table 2**	Jun. 11, 2025

Contact Us

PHISON ELECTRONICS
No. 1, Qunyi Road,
Zhunan Township,
Miaoli County 35059, Taiwan

Phone: +886-37-586-986
Fax: +886-37-586-866
https://www.phison.com/zh-tw/

About Us

Phison Electronics Corporation was established in November 2000 in Hsinchu, Taiwan. Starting with the world's first single-chip USB flash drive IC, Phison is now a market leader in NAND Flash controllers and applications including USB, SD, eMMC, PATA, SATA, PCIe and UFS. The company has shipped over 600 million controllers worldwide yearly and topped US 1.3 billion dollars in sales revenue. As a NAND flash total solution provider, Phison also offers system and OEM/ODM services for major brand names.

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PREFACE

About this Document

This document is to describe the PCIe Gen6 Redriver IC and the corresponded control signals. In addition, it discusses how to apply the functions and illustrates the status register reported by these functions.

Definition of Acronyms and Abbreviations

All acronyms and abbreviations used in place of the full definition in this document are listed in Table 1 below:

Table 1: Definition of Acronyms and Abbreviations

Item	Definitions
AIC	Add-In Card
EP	Endpoint
EQ	Equalization
EVB	Evaluation Board
FEXT	Far-End Cross Talk
FG	Flat Gain
NEXT	Near-End Cross Talk
PCIe	Peripheral Component Interconnect Express
RC	Root Complex
RX	Receiver
SL	Stripline
TX	Transmitter

1. OVERVIEW

1.1 General Description

The Phison PS7161 is a 4-channel high performance linear Redriver IC designed for Peripheral Component Interconnect Express (PCIe) 6.0 applications that supports up to 64 Gbps data rate. The Redriver provides programmable equalization, output swing, and flat gain to optimize performance over a variety of physical mediums, such as PCB traces, and transmission cables.

The PS7161 featuring high frequency boosting, low channel-channel cross-talk, low additive jitter and low return loss makes the device almost a passive element in the link. The programmable setting can be applied easily by either pin control or I^2C control. With signal adjustment flexibility of I^2C Mode, each channel has a set of independent control pins to make signal optimization possible.

Phison's exclusive technology "PHiTUNE" with our own SSD is able to collect and demonstrate the compulsory data, such as lane margining and eye opening, on the GUI for users and further to help to save tremendous efforts on system tuning by converging Redriver parameters.

1.2 Features

- Compliant with PCIe Gen 6.0 Standard up to 64 Gbps interfaces
- Four-channel linear pure PCIe Gen6 Redriver IC
- EQ boosting up to 20 dB at 16 GHz
- Low-latency of 70ps
- Adjustable output linear swing, flat gain, and equalization via Pin control and I^2C
- 4 level I/O for EQ and Gain setting to reduce pin count
- Supports I^2C and Phison PHiTUNE Technology for proper EQ setting
- Automatic receiver detection
- Rate and coding agnostic
- Transparent to link training
- Supply voltage: 3.3V
- Junction temperature: -40°C ~ +125°C
- Case temperature: -40°C ~ +115°C
- Package: FCLGA40, 6 mm x 4 mm

1.3 Application

- Rack Server / Blade Server / Tower Server
- Server Motherboard
- Data Center
- Workstation
- Desktop PC / Motherboard

2. PIN CONFIGURATION AND FUNCTIONS

2.1 Package Top View

		40	39	38	37	36	35	34	33	32	31	30	29		
		RXN3	RXP3	GND	RXN2	RXP2	VCC	VCC	RXN1	RXP1	GND	RXN0	RXP0		
1	GND													GND	28
2	RSVD													SIDEBAND_EN/ SDA	27
3	LEQ/ AD2													SW/ SCL	26
4	PERST_N						GND							MODE	25
5	CLKREQ_N													HEQ1/ AD1	24
6	PD													HEQ0/ AD0	23
7	DONEn													FG/ READ_EN_N	22
8	GND													GND	21
		TXN3	TXP3	GND	TXN2	TXP2	VCC	VCC	TXN1	TXP1	GND	TXN0	TXP0		
		9	10	11	12	13	14	15	16	17	18	19	20		

Figure 1: Ball Map of PS7161

2.2 Pin Functions

Table 2: Control Signals

No.	Pin Name		I/O, TYPE	Description
	Pin Mode	I²C Mode		
25	MODE	MODE	I, 4level	2'b11 = Enable Pin Mode and disable receiver detection 2'b10 = Enable I²C Slave Mode and receiver detection 2'b01 = Enable I²C Master Mode and receiver detection 2'b00 = Enable Pin Mode and receiver detection
7	DONE	DONE	I/O, open drain	Pin Mode: The pin is not used. I²C Slave Mode: The pin is not used. I²C Master Mode : High = External EEPROM loading fails. Low = External EEPROM loading is done.
6	PD	PD	I/O, open drain	Tie High = Channel 0 to 3 power-down Tie Low = Channel 0 to 3 normal operation
23	HEQ0	AD0	I, 4level	Pin Mode: 4 level RX-EQ boost on channel 0 to 3 I²C Slave/Master Mode: setting bit0 & bit1
24	HEQ1	AD1	I, 4level	Pin Mode: 4 level RX-EQ boost on channel 0 to 3 I²C Slave/Master Mode: setting bit2 & bit3
3	LEQ	AD2	I, 4level	Pin Mode: 4 level RX-EQ boost on channel 0 to 3 I²C Slave/Master Mode: setting bit4 & bit5
22	FG	READ_EN_N	I, 4level	Pin Mode: 4 level Flat Gain on channel 0 to 3 I²C Slave Mode: This pin is not used. I²C Master Mode: Tie high: Disable Load EEPROM Tie low: Enable Load EEPROM
27	SIDEBAND_EN	SDA	I/O, open drain	Pin Mode: Tie high: Enable sideband function Tie low: Disable sideband function I²C Slave/Master Mode: I²C SDA data input
4	PERST_N	PERST_N	I, 4level	This Pin can be used when -> Pin Mode : SIDEBAND_EN = H -> I2C Mode : Enabled by writing I2C register PERST_N default connects to PERST# signal, PERST_N = H : Normal operation PERST_N = L : Reset This pin is not used when -> Pin Mode : SIDEBAND_EN = L -> I2C Mode : Disable by writing I2C register (Default)
5	CLKREQ_N	CLKREQ_N	I, 4level	This Pin can be used When -> Pin Mode : SIDEBAND_EN = H -> I2C Mode : Enabled by writing I2C register CLKREQ _N default connects to CLKREQ# signal, CLKREQ _N = H : Low power mode CLKREQ _N= L : Normal operation This pin is not used when

No.	Pin Name		I/O, TYPE	Description
	Pin Mode	I²C Mode		
				-> Pin Mode : SIDEBAND_EN = L -> I2C Mode : Disable by writing I2C register (Default)
26	SW	SCL	I, 4level	Pin Mode: 2 level TX-Swing on channel 0 to 3 I²C Slave/Master Mode: I²C SCL data input

Table 3: Analog Signals

No.	Pin Name	I/O, TYPE	Description
14.15.34.35	VCC	I/O, power	Power supply, the range is 3.3 V ±10%.
1.8.11.18.21. 28.31.38	GND	I/O ground	Ground supply
29	RXP0	I	High-speed differential receiver signals of channel 0
30	RXN0	I	High-speed differential receiver signals of channel 0
32	RXP1	I	High-speed differential receiver signals of channel 1
33	RXN1	I	High-speed differential receiver signals of channel 1
36	RXP2	I	High-speed differential receiver signals of channel 2
37	RXN2	I	High-speed differential receiver signals of channel 2
39	RXP3	I	High-speed differential receiver signals of channel 3
40	RXN3	I	High-speed differential receiver signals of channel 3
9	TXN3	O	High-speed differential transmitter signals of channel 3
10	TXP3	O	High-speed differential transmitter signals of channel 3
12	TXN2	O	High-speed differential transmitter signals of channel 2
13	TXP2	O	High-speed differential transmitter signals of channel 2
16	TXN1	O	High-speed differential transmitter signals of channel 1
17	TXP1	O	High-speed differential transmitter signals of channel 1
19	TXN0	O	High-speed differential transmitter signals of channel 0
20	TXP0	O	High-speed differential transmitter signals of channel 0

3. SPECIFICATIONS

3.1 Absolute Maximum Ratings

Table 4: Absolute Maximum Ratings

		MIN	MAX	UNIT
VCC_{ABSMAX}	Supply Voltage	-0.5	3.6	V
$VIO_{COMS,ABSMAX}$	3.3V LVCMOS and Open Drain I/O voltage	-0.5	3.6	V
$VIO_{4LVL,ABSMAX}$	4-level Input I/O voltage	-0.5	2.75	V
$VIO_{HS-RX,ABSMAX}$	High-speed I/O voltage (RXnP, RXnN)	-0.5	3.2	V
$VIO_{HS-TX,ABSMAX}$	High-speed I/O voltage (TXnP, TXnN)	-0.5	2.75	V
$T_{J,ABSMAX}$	Junction temperature		150	°C
T_{STORE}	Storage temperature range	-65	150	°C
V_{ESD}	HBM Mode	-2000	2000	V
	CDM Mode	-250	250	V

☞ Stresses beyond the Absolute Maximum Ratings may cause permanent damage to the device. This list only indicates the stress ratings; the functional operation of the device under or beyond these conditions is not indicated in the Recommended Operating Conditions. Exposure to absolute maximum rating conditions for extended periods of time may affect the reliability of the device.

3.2 Recommended Operating Conditions

Table 5: Recommended Operating Conditions

			MIN	TYP	MAX	UNIT
VCC	Supply Voltage to Ground		3.0	3.3	3.6	V
$T_{VCCRAMP}$	Ramp Time of Supply Voltage	From 0 V to 3.0V	0.1		100	ms
T_{JUN}	Junction Temperature of Device		-40		125	°C
T_c	Case Temperature of Device		-40		115	°C
Data Rate			1		32	Gbps

3.3 DC Electrical Characteristics

Table 6: DC Electrical Characteristic List

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power						
I_{ACT}	Device current consumption when all four channels are active	All four channels enabled		270		mA
I_{IDLE}	Device current consumption in Electrical Idle Mode	All four channels in Electrical Idle Mode		28.9		mA
I_{LPM}	Device current consumption when all four channels are low power (by CLKREQ_N)	All four channels in Low Power Mode		3.07		mA
I_{STBY}	Device current consumption in Stand-by Mode (PD_*=H)	All four channels in Stand-by Mode		2.67		mA
VCC	Power supply voltage		3	3.3	3.6	V
V_{REG}	Internal regulator output		1.08	1.2	1.32	V
Receiver						
Z_{RX-DC}	Rx DC Single-Ended Impedance			50		Ω
$Z_{RX-DIFF-DC}$	Rx DC Differential Impedance			100		Ω
Transmitter						
$Z_{TX-DIFF-DC}$	DC Differential Tx Impedance	Impedance of Tx during active signaling		100		Ω
$V_{TX-DC-CM}$	Tx DC Common Mode Voltage (SW=00)			2.7		V
4 Level IO Electrical Characteristics						
V_{IH}	Input High Voltage	Input pin is connected to VCC	0.92*VCC	VCC	VCC+0.3	V
V_{IF}	Input Floating Voltage	Input pin is left floating (Open)	0.65*VCC	0.7*VCC	0.75*VCC	V

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IR}	Input Rext Voltage	Rext 100 kohm must be between pin and VSSK	0.25*VCC	0.36*VCC	0.5*VCC	V
V_{IL}	Input Low Voltage	Input pin is connected to VSSK	-0.3	VSS	0.08*VCC	V
Rext	External Resistor for VIR	Rext is connected to VSSK (±5%)	95	100	105	Kohm
I_{IH}	High−level input current				50	uA
I_{IL}	Low−level input current		-50			uA
GPIO Electrical Characteristics						
V_{IN}	PAD Voltage of Input Mode		-0.3		3.63	V
V_{IH}	Input High Voltage		0.7*VCC		VCC+0.5	V
V_{IL}	Input Low Voltage		-0.5		0.3*VCC	V
V_{OL}	Low-level output voltage for open-drain signals	open-drain at 3 mA sink current	0		0.4	V
$I_{IN\_power\ on}$	Input Leakage Current with Power on	V_{IN} = 0~3.63V VCC = 2.7~3.63V	-10		10	uA
$I_{IN\_power\ off}$	Input Leakage Current with Power off	V_{IN} = 0~3.63 VCC = 0V	-10		10	uA

☞ Use Schmitt Trigger for de-glitch function. In typical cases, the Vih is 0.60*VCC, and the Vil is 0.40*VCC.

3.4 High Speed Electrical Characteristics

Table 7: High Speed Electrical Characteristic List

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{pd}	Input-to-output latency (propagation delay) through a channel	Measured by observing propagation delay during Low-to-High or High-to-Low transition		70		ps
V_{noise_input}	Input-Referred Noise	Measured with minimum EQ boosting setting. 100MHz to 16GHz		0.62		mV_{rms}
		Measured with maximum EQ boosting setting. 100MHz to 16GHz.		0.53		
V_{noise_output}	Output-Referred Noise	Measured with minimum EQ boosting setting. 100MHz to 16GHz		0.7		mV_{rms}
		Measured with maximum EQ boosting setting. 100MHz to 16GHz.		2.03		
$EQ_{GAIN16G}$	High-frequency EQ boost @ 16 GHz	Measured with maximum EQ boosting setting. Boost is defined as the gain at 16 GHz relative to 100MHz.		20.8		dB
$EQ_{GAINVAR,max}$	Maximum EQ boost variation	Measured with maximum EQ boosting setting and 0dB DC gain setting. Boost is defined as the gain at 16 GHz relative to 100MHz.	-3		+2	dB
$DC_{GAINVAR,max}$	Maximum DC gain variation	Measured with minimum EQ boosting setting and 0dB DC gain setting. Boost is defined as the gain at 16 GHz relative to 100MHz.	-1		+1.5	dB
RL_{RX_DIFF}	Input differential return loss	100 MHz to 16 GHz		-12		dB
RL_{RX_COM}	Input Common-Mode return loss	100 MHz to 16 GHz		-8		dB
XT_{RX}	Receiver side isolation	100 MHz to 16 GHz		-50		dB

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
RL_{TX_DIFF}	Output differential return loss	100 MHz to 16 GHz		-12		dB
RL_{TX_COM}	Output Common-Mode return loss	100 MHz to 16 GHz		-8		dB
XT_{TX}	Transmitter side isolation	100 MHz to 16 GHz		-50		dB
V_{1dB_100M}	-1dB compression point of output swing (@100 MHz)	FG<1:0>=11, SW<2:0>=111, HFPK<3:0>=LFPK<3:0>=1111		1550		mV_{ppd}
V_{1dB_16G}	-1dB compression point of output swing (@16 GHz)	FG<1:0>=11, SW<2:0>=111, HFPK<3:0>=LFPK<3:0>=1111		1630		mV_{ppd}

3.5 SMBUS/I²C Timing Characteristics

3.5.1 I²C Slave for Standard/Fast Mode

Table 8: I²C Slave for Standard/Fast Mode

SYMBOL	PARAMETER	MIN	TYPE	MAX	UNIT
	SDA, SCL Input Voltage(High-Level)	0.7*VCC	--	--	V
	SDA, SCL Input Voltage(Low-Level)	--	--	0.3*VCC	
F_{SCL}	SCL Clock Rate	70	--	100/400	KHz
T_{HD_STA}	Hold Time START Condition	0.6	--	--	uS
T_{LOW}	Low Period of the SCL Clock	1.3	--	--	uS
T_{HIGH}	High Period of the SCL Clock	0.6	--	--	uS
T_{HD_DAT}	Data Hold Time	0	--	--	uS
T_{SU_DAT}	Data Set-Up Time	100	--	--	nS
T_{SU_STO}	Set-Up Time for STOP Condition	0.6	--	--	uS
T_{SU_STA}	Set-Up Time for a Repeated START Condition	1.3	--	--	uS
T_R	Rising Time of both SDA and SCL Signals	--	--	300	nS
T_F	Falling Time of both SDA and SCL Signals	--	--	300	nS
I_{OL}	SDA and SCL Output Low Sink Current	2	--	--	mA

3.5.2 I²C Master Mode

Table 9: I²C Master Mode

SYMBOL	PARAMETER	MIN	TYPE	MAX	UNIT
F_{SCL}	SCL Clock Rate	0	--	300	KHz
T_{HD_STA}	Hold Time START Condition	0.6	--	--	uS
T_{LOW}	Low Period of the SCL Clock	1.3	--	--	uS
T_{HIGH}	High Period of the SCL Clock	0.6	--	--	uS
T_{HD_DAT}	Data Hold Time	0	--	--	uS
T_{SU_DAT}	Data Set-Up Time	100	--	--	nS
T_{SU_STO}	Set-Up Time for STOP Condition	0.6	--	--	uS
T_{BUF}	bus free time between a STOP and START condition	1.3			uS
T_{SU_STA}	Set-Up Time for a Repeated START Condition	0.6	--	--	uS
T_R	Rising Time of both SDA and SCL Signals	--	--	300	nS
T_F	Falling Time of both SDA and SCL Signals	--	--	300	nS
T_{VD_DAT}	Data Valid Time	-	-	900	ns
T_{VD_ACK}	Data Valid Acknowledge Time	-	-	900	ns

4. DETAILED DESCRIPTION

4.1 Overview

The PS7161 is a four-channel linear Redriver with multi-rate function. The four channels operate independently from one another and each channel can be configured in three ways:

- Pin Mode: device control configuration is done solely by strap pins. Pin Mode is expected to be good enough for many system implementation needs.
- I^2C Slave Mode: provides most flexibility. Requires I^2C master device to configure the PS7161 through writing to its slave address.
- I^2C Master Mode: device control configuration is read from external EEPROM. When the PS7161 finishes reading from EEPROM, it drives ALL_DONE_N pin LOW.

4.2 Function Block Diagram

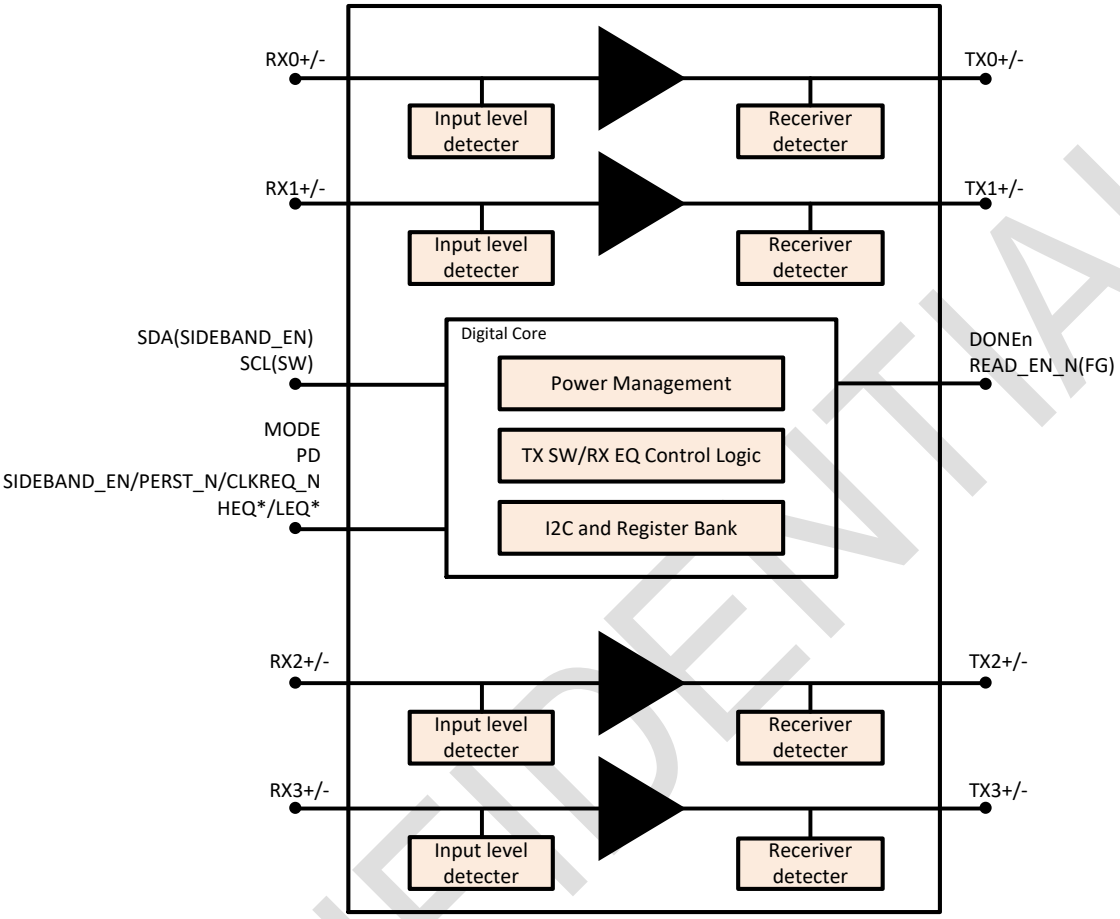


Figure 2: Block Diagram of PS7161

4.3 Feature Description

4.3.1 Four Level IO Control

Table 10: Four Level IO Control

PIN Control		
Symbol	Action	Code for 4-level
H	tie-to-VCC	11
F	floating	10
R	100kohm-to-VSS	01
L	tie-to-VSS	00

4.3.2 Linear Equalization

- Boosting for Pin Mode:

Table 11: EQ Boosting Setting of Pin Mode

Boosting [dB]	HEQ1_*,HEQ0_*	LEQ_*
2.3	L,L	L
3.2	L,R	L
4.3	L,F	R
5.4	L,H	R
7.2	R,L	R
8.2	R,R	R
9.5	R,F	R
10.3	R,H	R
12.0	F,L	F
13.0	F,R	F
13.9	F,F	F
14.6	F,H	F
16.3	H,L	H
18.6	H,R	H
19.9	H,F	H
20.8	H,H	H

- Flat gain for Pin Mode:

The recommended default setting is -0.2dB, i.e., FG pin is tied to VCC.

Table 12: Flat Gain Setting for Pin Mode

FG_*	Flat Gain [dB]
L	-2.0
R	-2.0
F	-0.2
H	-0.2

- Boosting for I²C Mode:

Table 13: EQ Boosting Setting for I²C Mode

Boosting [dB]	SYS_HFPK [DEC]	SYS_LFPK [DEC]	SYS_HFPK, SYS_LFPK [BIN]
2.3	0	2	0000,0010
3.2	1	3	0001,0011
4.3	2	4	0010,0100
5.4	3	5	0011,0101
7.2	4	5	0100,0101
8.2	5	5	0101,0101
9.5	6	5	0110,0101
10.3	7	7	0111,0111
12.0	8	8	1000,1000
13.0	9	8	1001,1000
13.9	10	10	1010,1010
14.6	11	10	1011,1010
16.3	12	12	1100,1100
18.6	13	13	1101,1101
19.9	14	14	1110,1110
20.8	15	14	1111,1110

- Flat gain for I²C Mode:

Table 14: Flat Gain Setting for I²C Mode

Flat Gain [dB]	SYS_FG [DEC]	SYS_FG [BIN]
-2.8	0	00
-2.0	1	01
-0.8	2	10
-0.2	3	11

4.3.3 Driver Swing (16GHz)

- Swing for Pin Mode:

Table 15: Swing Setting for Pin Mode

Swing Setting	
SW_*	Swing [mVppd]
H	1270
L	1050

- Swing for I²C Mode:

Table 16: Swing Setting for I²C Mode

Swing [mVppd]	SYS_SW [DEC]	SYS_SW [BIN]
1050	0	000
1150	1	001
1270	2	010
1380	3	011
1460	4	100
1490	5	101
1600	6	110
1630	7	111

4.3.4 Finite State Machine

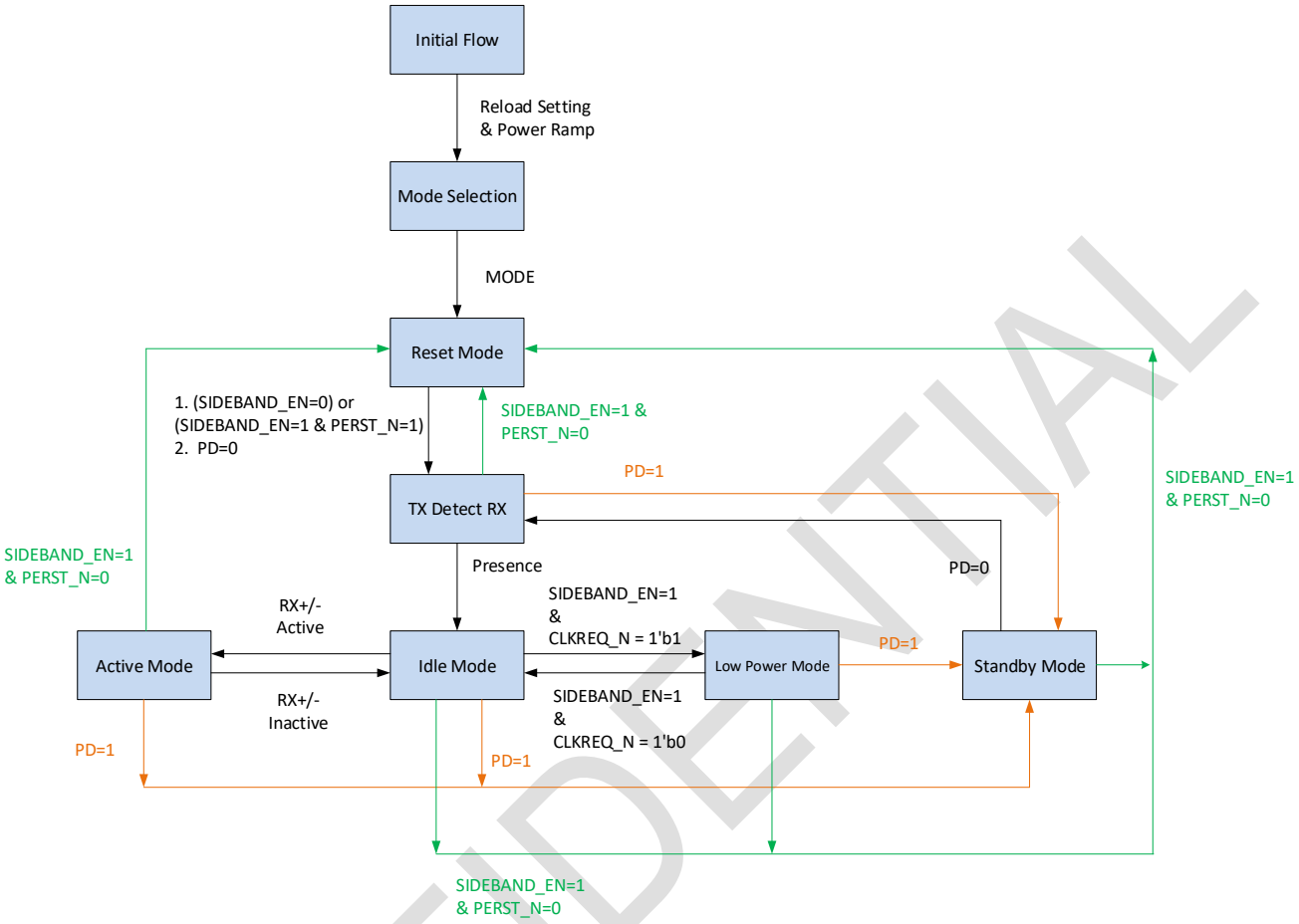


Figure 3: Finite State Machine

4.4 Device Functional Modes

4.4.1 Initial Flow

First, the device waits for the internal or external power supply to be stable. Second, the internal PMU reloads all initial settings from eFuse.

4.4.2 Mode Selection

The device checks that the GPIO setting can switch between Pin Mode and I^2C Mode.

4.4.3 Reset Mode

The device is in Reset Mode triggered by PRSNTB=1. In this mode, no connection is established in the PCIe system.

In this mode, the user has two options: (1) The PCIe state machine is disabled by SIDEBAND_EN=1, which means the device disables the PERST_N function. (2) The PCIe state machine is enabled by PD_0 and PD_1, which means the device is able to turn on/off lanes.

4.4.4 Active Mode

The device is in normal operation. In this mode, the device is working in transmission and receiving state.

4.4.5 Standby Mode

The device is in Standby Mode inactivating differential receivers. In this mode, the device provides basic low power state to reduce power consumption. It can map to LTSSM states including L0s, L1.0, L2, Disable and Hot Reset.

4.4.6 Low Power Mode

The device is in Low Power Mode (LPM) triggered by SIDBAND_EN=1 and CLKREQB=1. In this mode, the device provides an advanced low power state to reduce power consumption. It can map to LTSSM states of L1.1 and L1.2. The features are listed below:

- Switching to idle mode takes no more than 20μs.
- LPM is activated when CLKREQB=1 remains for more than 2μs.
- CPM L1 is not supported.
- TX Common Mode is maintained during LPM.
- The default setting is “enable” and can be disabled by I^2C or SIDEBAND_EN.

4.5 Programming

4.5.1 Configuration Register Type

Table 17: I²C for Fast Mode

Attribute	Description
RO	READ-ONLY register: the register bits are “read-only” and CANNOT be altered by software. Register bits may be initialized by hardware mechanisms such as pin strapping or serial EEPROM; however, IP Reset CANNOT clear the status of this register type.
RW	READ-WRITE register: the register bits are “read-write” and may either be set or cleared by software to the desired state.

4.5.2 Register Overview

Table 18: Address Map of the Control Register

Offset	Symbol	bit	Default Value	Attribute	Register Description
0x00	SYS_HFPK_0P	[7:4]	4'h0	RW	High Frequency Peak for Channel 0
	SYS_LFPK_0P	[3:0]	4'h5	RW	Low Frequency Peak for Channel 0
0x01	SYS_SW_0P	[6:4]	2'h0	RW	Output swing for Channel 0
	SYS_FG_0P	[1:0]	2'h3	RW	Flat gain for Channel 0
0x02	SYS_HFPK_1P	[7:4]	4'h0	RW	High Frequency Peak for Channel 1
	SYS_LFPK_1P	[3:0]	4'h5	RW	Low Frequency Peak for Channel 1
0x03	SYS_SW_1P	[6:4]	2'h0	RW	Output swing for Channel 1
	SYS_FG_1P	[1:0]	2'h3	RW	Flat gain for Channel 1
0x04	SYS_HFPK_2P	[7:4]	4'h0	RW	High Frequency Peak for Channel 2
	SYS_LFPK_2P	[3:0]	4'h5	RW	Low Frequency Peak for Channel 2
0x05	SYS_SW_2P	[6:4]	2'h0	RW	Output swing for Channel 2
	SYS_FG_2P	[1:0]	2'h3	RW	Flat gain for Channel 2
0x06	SYS_HFPK_3P	[7:4]	4'h0	RW	High Frequency Peak for Channel 3
	SYS_LFPK_3P	[3:0]	4'h5	RW	Low Frequency Peak for Channel 3
0x07	SYS_SW_3P	[6:4]	2'h0	RW	Output swing for Channel 3
	SYS_FG_3P	[1:0]	2'h3	RW	Flat gain for Channel 3
0x08	PHITUNE_SEL_0P	[7:4]	4'h4	RW	PHITUNE Tool Option
	PHITUNE_SEL_EN_0P	[0]	1'h0	RW	PHITUNE Tool Option
0x09	PHITUNE_SEL_1	[7:4]	4'h4	RW	PHITUNE Tool Option
	PHITUNE_SEL_EN_1	[0]	1'h0	RW	PHITUNE Tool Option
0x0A	PHITUNE_SEL_2P	[7:4]	4'h4	RW	PHITUNE Tool Option
	PHITUNE_SEL_EN_2P	[0]	1'h0	RW	PHITUNE Tool Option
0x0B	PHITUNE_SEL_3P	[7:4]	4'h4	RW	PHITUNE Tool Option
	PHITUNE_SEL_EN_3P	[0]	1'h0	RW	PHITUNE Tool Option

Offset	Symbol	bit	Default Value	Attribute	Register Description
0x0C-0X0F	Reserve	Reserve	Reserve	Reserve	Reserve
0x10	PD_CH_EN	[0]	1'b0	RW	Enable power down overrides through I²C/SMBus 0: Manual override disabled 1: Manual override enabled
0x11	Reserve	[7:4]	Reserve	Reserve	Reserve
	CH3_PD	[3]	1'h0	RW	Manual channel 3 power done
	CH2_PD	[2]	1'h0	RW	Manual channel 2 power done
	CH1_PD	[1]	1'h0	RW	Manual channel 1 power done
	CH0_PD	[0]	1'h0	RW	Manual channel 0 power done
0x12	DET_LOOP_CNT_3P_0P	[5:4]	2'h0	RW	txdetrx detecting counter for ch3 to ch0
	BYPASS_SQ_3P_0P	[1]	1'h0	RW	bypass detecting squelch for ch3 to ch0
	BYPASS_DET_3P_0P	[0]	1'h0	RW	bypass tx detecting rx ch for ch3 to ch0
0x13	Reserve	[7]	Reserve	Reserve	Reserve
	SIDEBAND_EN	[6]	1'h0	RW	SIDEBAND_EN
	Reserve	[5:0]	Reserve	Reserve	Reserve
0x14	Reserve	[7:0]	NA	R	Reserve
0x15	MPVERSION	[7:5]	3'h0	RW	record MP batch information (from eFuse)
	MPCODE	[4:0]	5'h00	RW	record MP product information (from eFuse)
0x16-0x17	Reserve	Reserve	Reserve	Reserve	Reserve

Reserve: Do NOT perform I²C rewrite.

4.5.3 Control and Configuration Interface

The PS7161 internal registers can be accessed through standard I²C protocol. The I²C slave address is determined at power-up based on the configuration of the HEQ0, HEQ1, LEQ pins in I2C Mode. The pin state is read on power-up, after the internal power-on reset signal is de-asserted.

There are 64 unique I²C slave addresses of 7'bit AD[6:0] that can be assigned to the device via the connected VSS or VCC on the HEQ0, HEQ1, LEQ pins as shown in Table 19. When multiple PS7161 devices are on the same I²C interface bus, each device must be configured with a unique I²C slave address.

Table 19: PS7161 I²C Slave Address Map

Pin Name	Pin Level	Slave Address[6:0]

HEQ0	Tie-to-VSS	AD[1:0]=2'b00
	Floating	AD[1:0]=2'b10
	100kohm-to-VSS	AD[1:0]=2'b01
	Tie-to-VCC	AD[1:0]=2'b11
HEQ1	Tie-to-VSS	AD[3:2]=2'b00
	Floating	AD[3:2]=2'b10
	100kohm-to-VSS	AD[3:2]=2'b01
	Tie-to-VCC	AD[3:2]=2'b11
LEQ_1	Tie-to-VSS	AD[5:4]=2'b00
	Floating	AD[5:4]=2'b10
	100kohm-to-VSS	AD[5:4]=2'b01
	Tie-to-VCC	AD[5:4]=2'b11

☞ slave address format: 0x08+AD[5:0]

4.5.4 I²C Register Control Interface

The PS7161 I²C slave address can be configured by 4-level input pins (HEQ0, HEQ1, LEQ). The I²C interface supports Standard Mode (100 kbps) and Fast Mode (400 kbps). The I²C bus transfer format is 31 ≥ m ≥ 0. Refer to Figure 4 and Figure 5 for timing definitions.

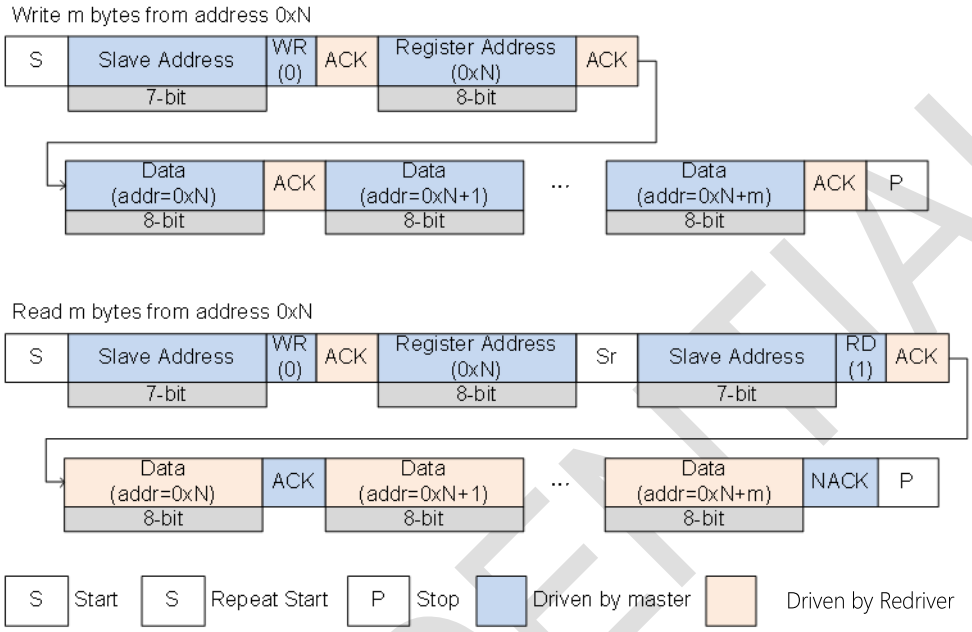


Figure 4: Data Transfer Format in F/S Mode

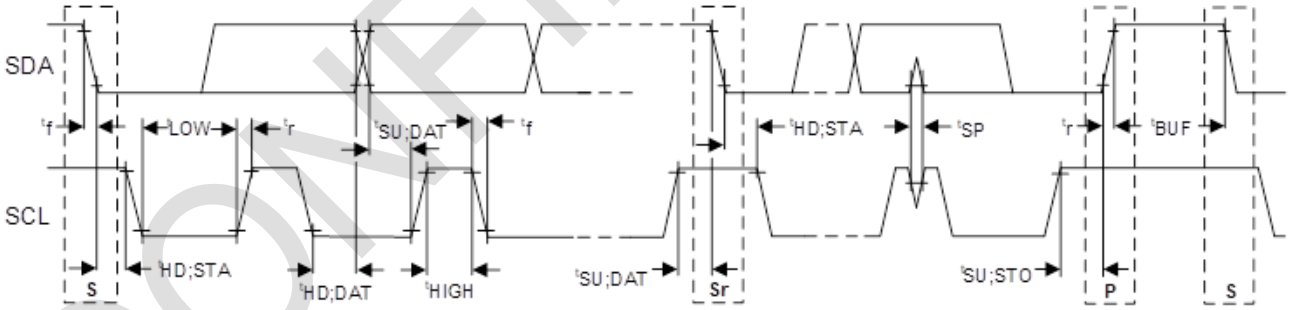


Figure 5: Definition of Timing for F/S Mode Devices on the I²C Bus

4.5.5 Power-On Sequence

When the 3.3V power source is stable, the redriver requires 10 ms to activate the internal circuit. During this period, please ensure that the I2C bus remains in an idle state. If the redriver is in I2C Mode and in an active state, it can receive and respond to commands from the I2C master. Ensure that the configuration of the redriver registers takes place between 'redriver active' and 'PERST# rising.' Furthermore, if you need to configure 'SIDEBAND_EN,' please ensure it is sent at the end of the command packet, and disable the I2C configuration function after issuing this command.

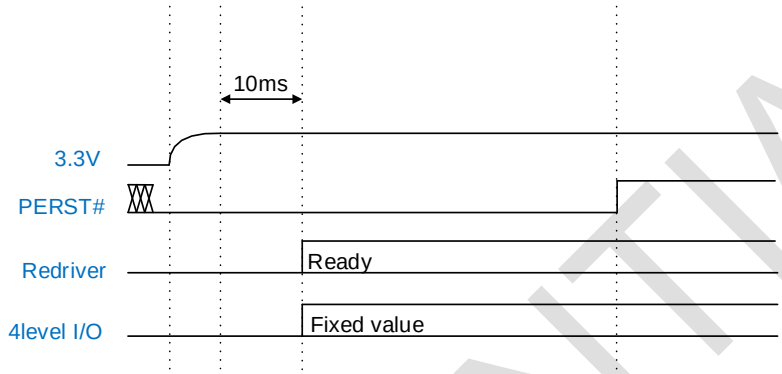


Figure 6: Power On Sequence for PS7161 Pin Mode

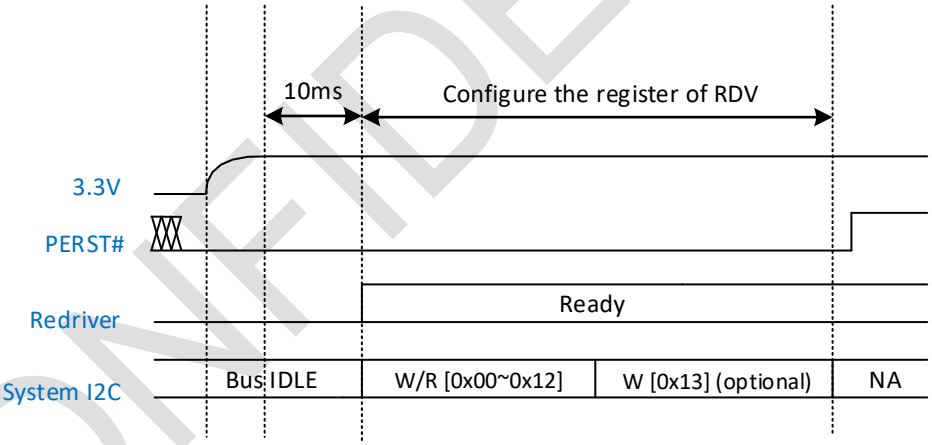


Figure 7: Power On Sequence for PS7161 I^{2}C Mode

4.5.6 The “Detect counter” feature of the Redriver RX detection function is enabled by default in compatibility test.

To enhance the compatibility during the RX detection between the Redriver and other PCIe devices, it is recommended to enable the “Detect Counter” feature by default.

This can be achieved by configuring the following register settings as below:

• Offset 0x12 = 0x10

5. APPLICATION AND IMPLEMENTATION

5.1 Typical Applications

5.1.1 Pin Mode Configuration

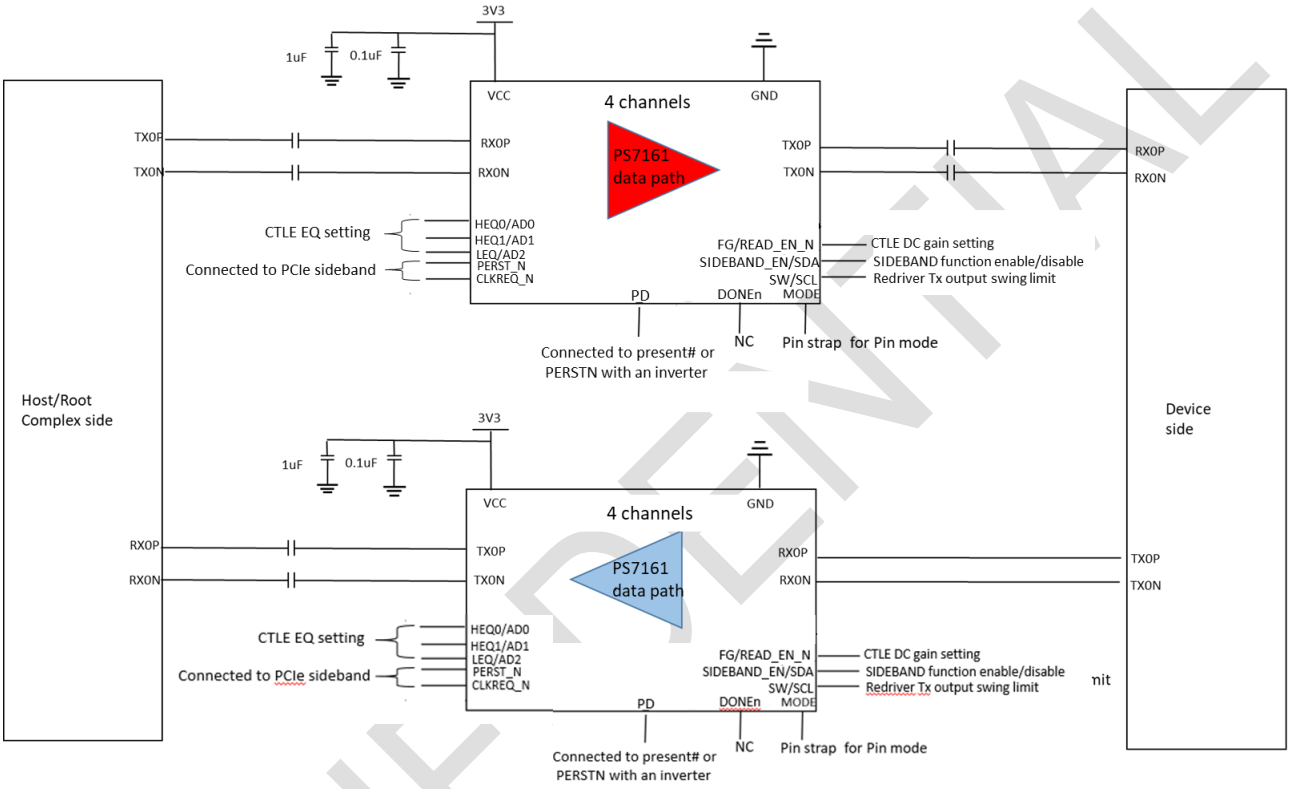


Figure 8: Simplified Schematic for Pin Mode Configuration

5.1.2 I²C Slave Mode Configuration

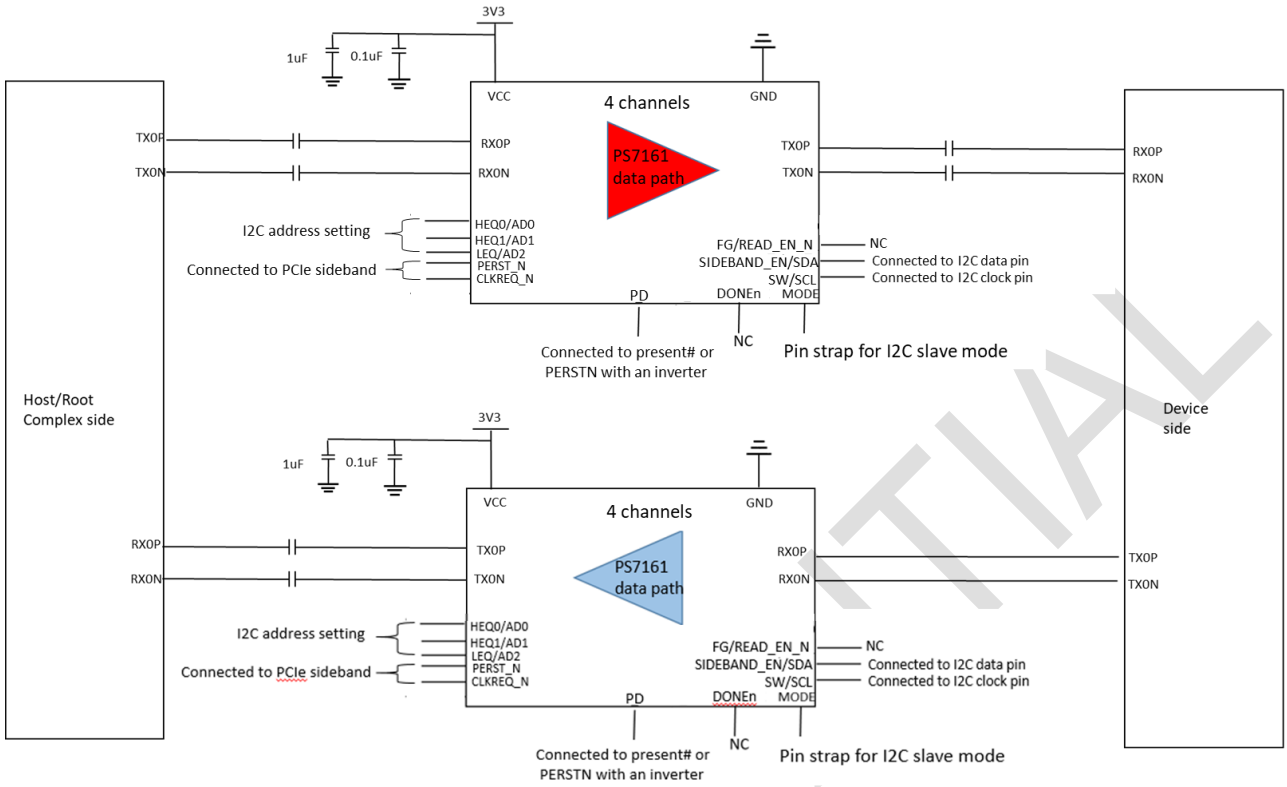


Figure 9: Simplified Schematic for I²C Slave Configuration

5.1.3 I²C Master Mode Configuration

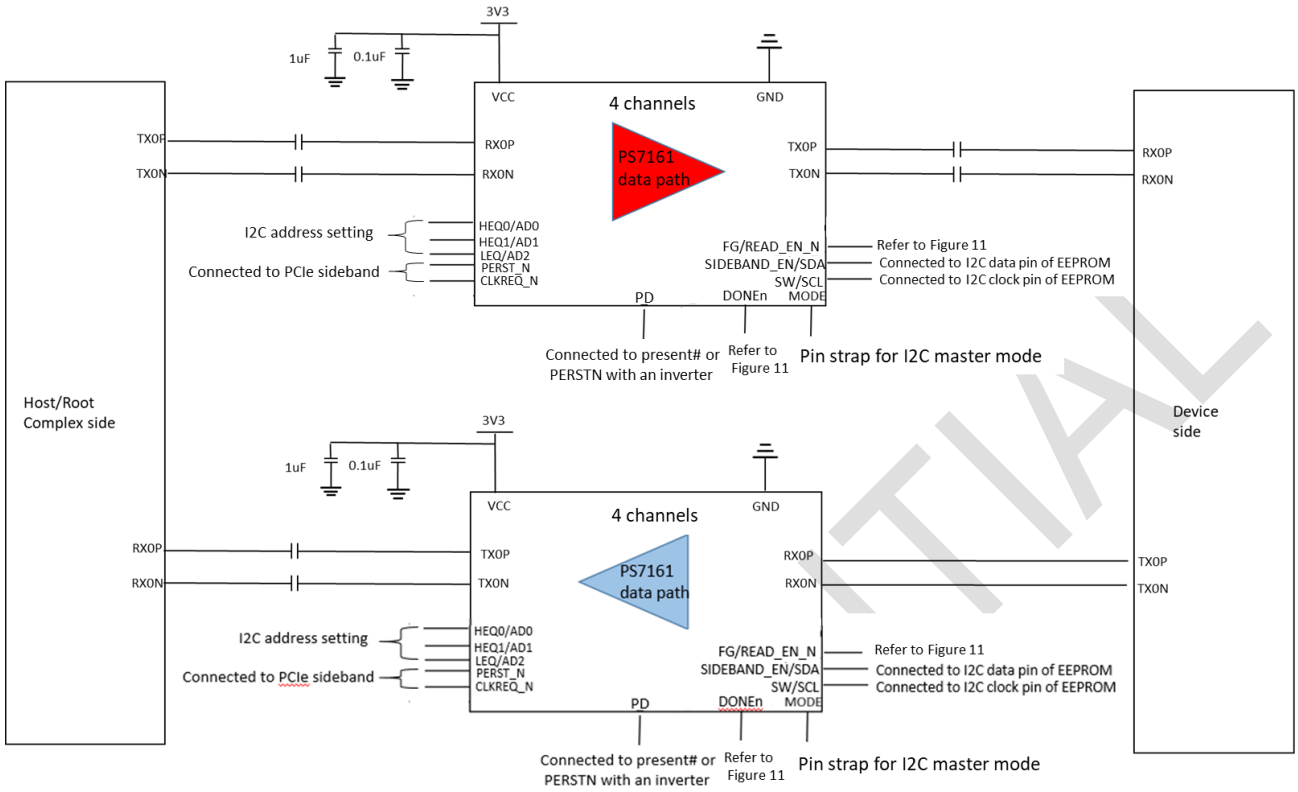


Figure 10: Simplified Schematic for I²C Master Mode Configuration

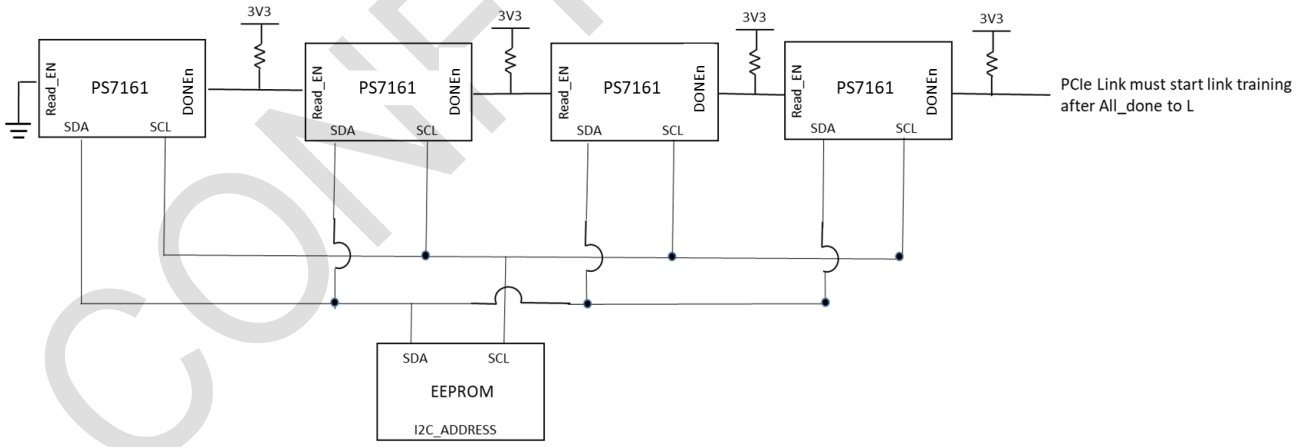


Figure 11: Simplified Schematic for I²C Master Mode_2 Configuration

5.2 I²C Master Mode

In PS7161/7162, I²C Master Mode is configured by the user external EEPROM to support the Redriver setting.

5.2.1 Main I²C Master Mode Pin Setting

1. “Mode” pin:
For PS7161, connected to 100K Ohm-Gnd.
For PS7162, connected to 50K Ohm-Gnd.

2. “Read_En_N” pin:
Connected to Gnd to enable EEPROM Read.

3. “SDA/SCL” pin:
Connected to the I²C Bus of EEPROM (EEPROM is I²C slave and PS7161/PS7162 is I²C master.)

4. “AD0~2” pin (4-level IO):
A four-level IO setting configures address mapping for different types of EEPROM.
Details are to be described in the following chapter.

Figure 12 is an example of the connection between single PS7161 and EEPROM.

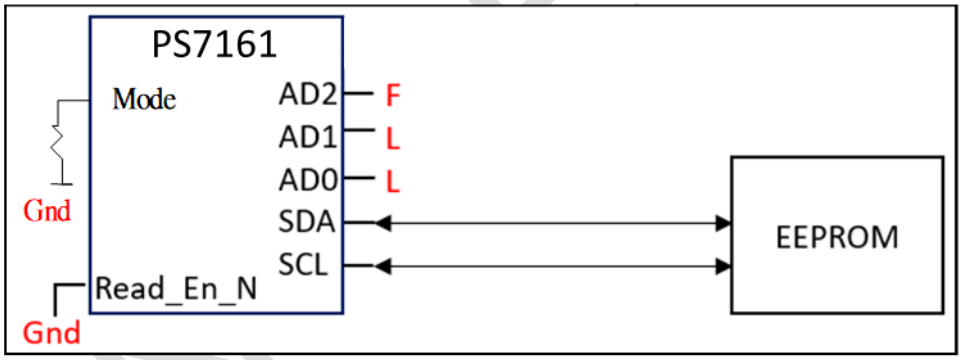


Figure 12: Connection Between Single PS7161 and EEPROM

5.2.2 Four-Level I/O

The 4-level IO function for “AD0~2” pins is illustrated in Figure 13. Each “AD0~2” pin generates two internal logic values (ad0/ad1).

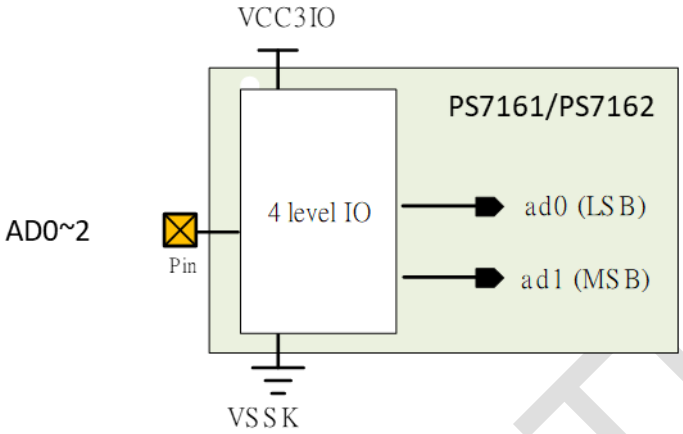


Figure 13: 4-level IO Function for “AD0~2”

The 4-level IO input setting and the internal logic value (ad0/ad1) are shown in Table 20.

Table 20: 4-level IO Input Setting

	Each AD0~2 pin input setting			
Internal logic value	(L) Connected to VSSK	(R) Rext 100kohm between pin and VSSK	(F) Floating (Open)	(H) Connected to VCC3IO
ad1 (MSB)	0	0	1	1
ad0 (LSB)	0	1	0	1

5.2.3 PS7161 I²C Master Mode Pin Settings

Table 21 shows PS7161 I²C Master Mode pin settings where different numbers of Redrivers are used.

Table 21: PS7161 I²C Master Mode Pin Settings

PS7161 Pin Name	Pin Strap	
Mode	100KOhm-Gnd	
Read_En_N	L (Gnd)	
SDA/SCL	Connect to EEPROM	
AD2	L (Gnd)	H/F
AD1	L (Gnd)	H/F/R/L
AD0	H/F/R/L	H/F/R/L
Note	Support up to 4*PS7161	Support up to 32*PS7161

5.2.4 PS7162 I²C Master Mode Pin Settings

Table 22 shows PS7162 I²C Master Mode pin settings where different numbers of Redrivers are used.

Table 22: PS7162 I²C Master Mode Pin Settings

PS7162 (CH3-0) Pin Name	PS7162 (CH7-4) Pin Name	Pin Strap	
Mode		50K Ohm-Gnd	
Read_En_N		L (Gnd)	
SDA/SCL		Connect to EEPROM	
AD2		L (Gnd)	H/F
AD1_0	AD1_1	L (Gnd)	H/F/R/L
AD0_0	AD0_1	H/F/R/L	H/F/R/L
Note		Support up to 2*PS7162	Support up to 16*PS7162

When I²C Master Mode is enabled, PS7161/PS7162 automatically load EEPROM and apply the setting to each Redriver channel after the power is on. PS7161/PS7162 also provide the CRC protection to check whether the EEPROM read data is correct or not. For EEPROM usage, CRC generation, and result checking, refer to the following chapters.

5.3 EEPROM Programming Guide

To support various EEPROMs, PS7161/PS7162 provide 2 types of address mapping for user to set “AD0~2”.

Table 23 shows the mapping between address strap pins (AD0~2) and the 2 types of EEPROM. Follow the table to configure the setting for both PS7161/7162 with different types of EEPROM. If AD2 pin is set, different types of EEPROM can be configured.

Table 23: Address Strap Pins Mapping for EEPROM

Redriver/Channel		Redriver Pin Name					
PS7161		AD2		AD1		AD0	
PS7162	PS7162 Channel 0-3	AD2		AD1_0		AD0_0	
	PS7162 Channel 4-7			AD1_1		AD0_1	
Address Strap Pin Bit Description		A5 (ad1) (MSB)	A4 (ad0) (LSB)	A3 (ad1) (MSB)	A2 (ad0) (LSB)	A1 (ad1) (MSB)	A0 (ad0) (LSB)
Type1 Pin Setting		L		L		H/F/R/L	
Type1 Address Bit		1	X	X	X	EEPROM data address Bit7	EEPROM data address Bit6
Type2 Pin Setting		H/F		H/F/R/L		H/F/R/L	
Type2 Address Bit		0	EEPROM data address Bit10	EEPROM data address Bit9	EEPROM data address Bit8	EEPROM data address Bit7	EEPROM data address Bit6

Note: Phison supports 2 types of EEPROM.

5.3.1 Address Mapping Type 1

Set AD2 = 0/x.
Supports 4 Target Address in single EEPROM, each space = 64B.
Supports EEPROM I²C ID = 0x50 (fixed).
Supports each EEPROM up to maximum capacity = 256B.

Table 24 shows I²C command sequence for type1 EEPROM. PS7161/PS7162 follow the command sequence to load data from EEPROM.

Table 24: I²C Command Sequence for Type1 EEPROM

EEPROM I²C ID[7:1]							
bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
1	0	1	0	0	0	0	R/W
EEPROM I²C data address [7:0]							
bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
A1 (ad1) (MSB)	A0 (ad0) (LSB)	EEPROM address[5]	EEPROM address[4]	EEPROM address[3]	EEPROM address[2]	EEPROM address[1]	EEPROM address[0]

5.3.2 Address Mapping Type 2

Set AD2= 1/x.
Supports 32 Target Address in single EEPROM, each space = 64B.
Supports EEPROM I²C ID = 0xA (only 4 bits, ID[7:4], are useful.)
Supports each EEPROM up to maximum capacity = 2048B.

Table 25 demonstrates I²C command sequence for type2 EEPROM. PS7161/7162 follow the command sequence to load data from EEPROM.

Table 25: I²C Command Sequence for Type2 EEPROM

EEPROM I²C ID [7:1]							
bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
1	0	1	0	A4 (ad0) (LSB)	A3 (ad1) (MSB)	A2 (ad0) (LSB)	R/W
EEPROM I²C data address [7:0]							
bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
A1 (ad1) (MSB)	A0 (ad0) (LSB)	EEPROM address[5]	EEPROM address[4]	EEPROM address[3]	EEPROM address[2]	EEPROM address[1]	EEPROM address[0]

5.3.3 EEPROM Preparation

To prepare for EEPROM, identify the architecture as the first step. The key points are listed below:

- Each PS7161 needs 64B space with:
  16 bytes register setting for all 4-channel Redrivers +
  1 byte CRC code (generated from 20 bytes above +
  15 bytes reserved region (all data should be set as "0x00") +
  32 bytes repeating all the data above (backup use for the second code loading if the first 32B CRC is wrong.)
- In the cases where multiple PS7161 Redrivers are used, the general concept for each is the same, but the address strap pins (AD0~2) should be different, so as to locate the different address. Each 64B is appended one after another from lower 64B to higher ones.
- In the cases where single or multiple PS7162 Redrivers are used, the concept for each (PS7161 die) is the same but the address strap pins (AD0~2) should be different, in order to locate the different address. Each 64B is appended one after another from lower 64B to higher ones.

For 20-byte register setting, refer to the register table.

- EQ setting for each channel (decided by the user)
- Swing setting for each channel (default and fixed)
- Flat gain setting for each channel (default and fixed)

Figure 14 shows the steps to preparing for EEPROM.

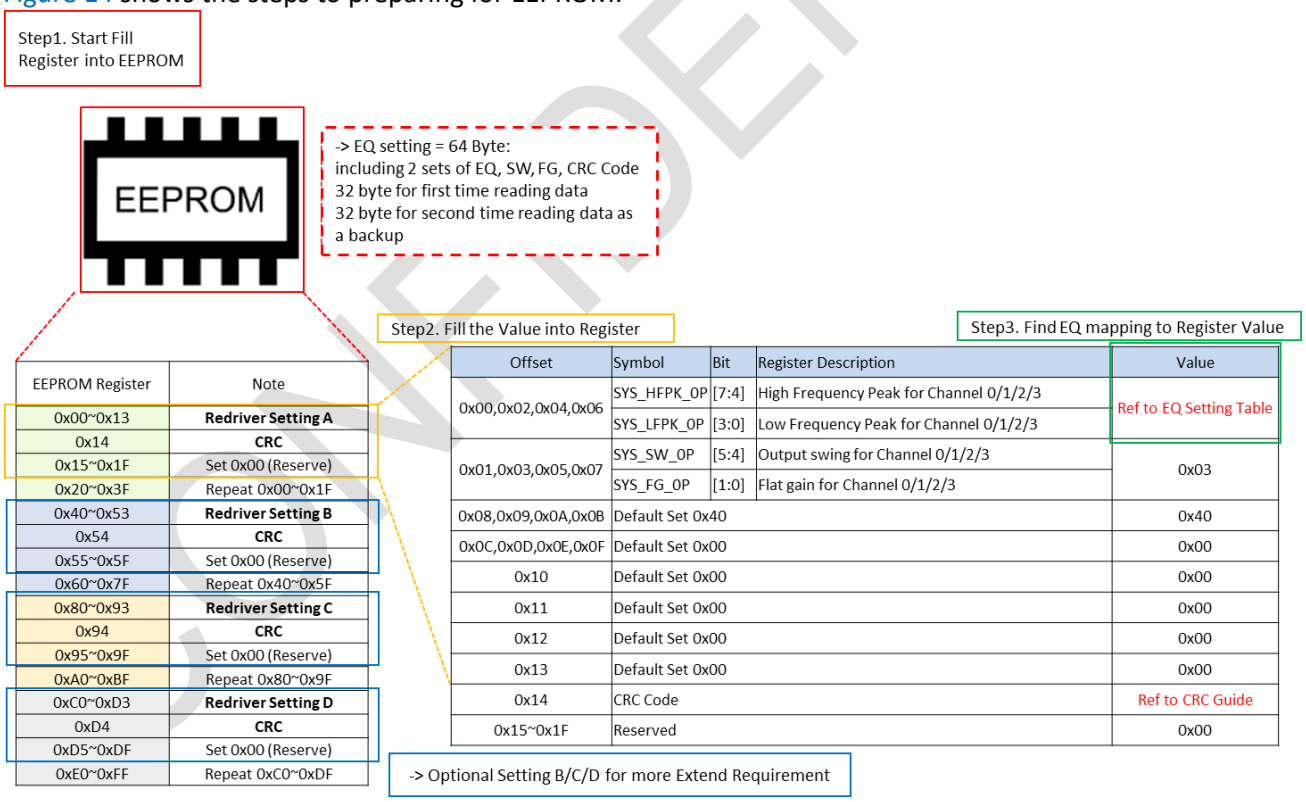


Figure 14: Steps for Generating CRC Code

Simply fill up the EQ setting for each channel. Figure 15 shows the EEPROM address offset and EQ boost mapping table.

Offset	Symbol	Bit	Register Description	Value
0x00	SYS_HFPK_0P	[7:4]	High Frequency Peak for Channel 0	Ref to EQ Setting Table
	SYS_LFPK_0P	[3:0]	Low Frequency Peak for Channel 0	
0x02	SYS_HFPK_1P	[7:4]	High Frequency Peak for Channel 1	Ref to EQ Setting Table
	SYS_LFPK_1P	[3:0]	Low Frequency Peak for Channel 1	
0x04	SYS_HFPK_2P	[7:4]	High Frequency Peak for Channel 2	Ref to EQ Setting Table
	SYS_LFPK_2P	[3:0]	Low Frequency Peak for Channel 2	
0x06	SYS_HFPK_3P	[7:4]	High Frequency Peak for Channel 3	Ref to EQ Setting Table
	SYS_LFPK_3P	[3:0]	Low Frequency Peak for Channel 3	

Confirm the desired EQ Boost, and look for the matching value in the Table. Then fill up to EEPROM content file at proper offset address

Step3. Find EQ mapping to Register Value

TBD

Figure 15: EEPROM Address Offset and EQ Boost Mapping Table

The CRC code generator, named "ps7161_PS7162_CRC_Generator.xlsx," helps to generate 1Byte CRC code for 20 Byte setting data. Figure 16 shows the steps to generating CRC code.

- Detail for EEPROM CRC Code

Step 1. Open File "PS7161_PS7162_CRC_Generator"

PS7161_PS7162_CRC_Generator

Step 2. Fill EEPROM Setting 0x00~0x13 in the Excel Table

PS7161/PS7162 and EEPROM Register Offset	CRC Parameter (Fixed) Pre Input	Register Setting (Fill LRD Setting Here)	CRC Parameter (Fixed) Output
0x00	FF	95	A6
0x01	A6	3	EE
0x02	EE	95	21
0x03	21	3	55
0x04	55	95	FC
0x05	FC	3	77
0x06	77	95	A9
0x07	A9	3	5A
0x08	5A	40	4
0x09	4	40	AA
0x0A	AA	40	C7
0x0B	C7	40	BB
0x0C	BB	0	DD
0x0D	DD	0	22
0x0E	22	0	55
0x0F	55	0	2D
0x10	2D	0	E1
0x11	E1	0	44
0x12	44	0	AA
0x13	AA	0	5A
0x14	5A		99
	↑0x14 CRC Here		

confirm EQ,SW,FG setting and fill up to proper address offset, CRC Code is generated by Excel automatically, then user needs to fill up to EEPROM content file

EEPROM Register	Note
0x00~0x13	**Redriver Setting A**
0x14	**CRC**
0x15~0x1F	Set 0x00 (Reserve)
0x20~0x3F	Repeat 0x00~0x1F
0x40~0x53	**Redriver Setting B**
0x54	**CRC**
0x55~0x5F	Set 0x00 (Reserve)
0x60~0x7F	Repeat 0x40~0x5F
0x80~0x93	**Redriver Setting C**
0x94	**CRC**
0x95~0x9F	Set 0x00 (Reserve)
0xA0~0xBF	Repeat 0x80~0x9F
0xC0~0xD3	**Redriver Setting D**
0xD4	**CRC**
0xD5~0xDF	Set 0x00 (Reserve)
0xE0~0xFF	Repeat 0xC0~0xDF

Step3. Get CRC Code from Table and Fill in EEPROM Offset 0x14

EEPROM Word Address	+00	+01	+02	+03	+04	+05	+06	+07	+08	+09	+0A	+0B	+0C	+0D	+0E	+0F
000	95	03	95	03	95	03	95	03	40	40	40	40	00	00	00	00
010	00	00	00	00	5A	00	00	00	00	00	00	00	00	00	00	00
020	95	03	95	03	95	03	95	03	40	40	40	40	00	00	00	00
030	00	00	00	00	5A	00	00	00	00	00	00	00	00	00	00	00

-> Repeat Steps for Setting A to "get and set Setting B/C/D" if needed

Figure 16: Steps for Generating CRC Code

To stabilize the performance of EEPROM data loading, PS7161/PS7162 provide the second chance for loading if error occurs in the first 20B CRC. The second 20B+CRC is the same as the first, yet applies to the backup data. CRC checking result is stored in the register table below. If EEPROM loading is done, PS7161/PS7162 enters I^2C Slave Mode automatically. Read the CRC result or other user registers via I^2C host if debugging is required.

Table 26 shows the EEPROM loading status record for debugging.

Table 26: EEPROM Loading Status Record for Debugging

Address	Register name	Bit Number	Default Value	Type	Description
0x16	i2m_fail	4	1'h0	R	EEPROM ID mismatch
0x16	EECFG_FAIL_2	3	1'h0	R	EEPROM load fail (second time)
0x16	EECFG_CMPLT_2	2	1'h0	R	EEPROM load setting complete (second time)
0x16	EECFG_FAIL_1	1	1'h0	R	EEPROM load fail (first time)
0x16	EECFG_CMPLT_1	0	1'h0	R	EEPROM load setting complete (first time)

The EEPROM CRC checking results are listed below.

- When the data is loading, and if I^2C ID to EEPROM is abnormal, i2m_fail is set to 1. Check whether "AD0~2" setting matches the current EEPROM.
- If EECFG_CMPLT_1 = 1 and EECFG_FAIL_1 = 0, it indicates that the first 20 byte is loaded and the data is correct.
- If EECFG_CMPLT_1 = 1 and EECFG_FAIL_1 = 1, it means that the first 20 byte is loaded and that there is an error in data. In this case, the second loading for the backup data is triggered.
- If EECFG_CMPLT_2 = 1 and EECFG_FAIL_2 = 0, it represents that the second 20 byte is loaded and that the data is correct.
- If EECFG_CMPLT_2 = 1 and EECFG_FAIL_2 = 1, it shows that the second 20 byte is loaded and that there is an error in data, which means that EEPROM loading fails and EEPROM might be damaged and needs repairing or swapping.

Figure 17 shows the I^2C Master Mode power on and sequence of loading EEPROM.

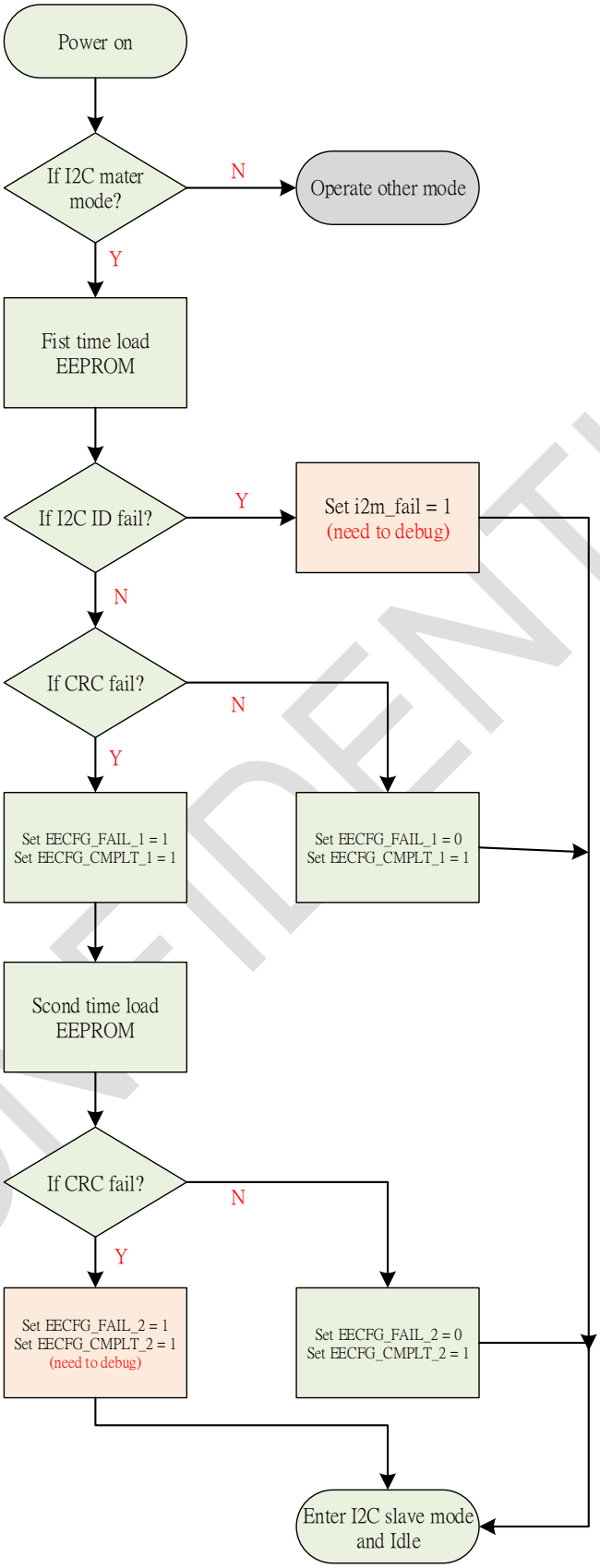


Figure 17: I²C Master Mode Power On and Sequence of Loading EEPROM

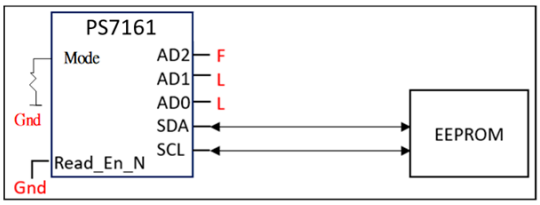
5.3.4 Example of I²C Master Mode

In this section, examples of I²C Master Mode are provided and the detail configuration and setting for different cases are described.

Example 1: Single PS7161 with single EEPROM
In this case, EEPROM capacity minimum requirement = 64B.

Example 1 – PS7161*1 to 1 EEPROM

Block Diagram



PS7161 Pin Strap

PS7161 Pin Name	Pin Setting
AD2	L (Gnd)
AD1	L (Gnd)
AD0	L (Gnd)
Note.	Read EEPROM 0x00~0x3F

-> tuning Address Pin Strap to read EEPROM EQ setting at proper address offset

PS7161 Register
0x00~0x13 (Setting)

EEPROM Register	Note
0x00~0x13	PS7161 Setting
0x14	CRC
0x15~0x1F	Set 0x00 (Reserve)
0x20~0x3F	Repeat 0x00~0x1F

Figure 18: Single PS7161 with Single EEPROM

Example 2: Four PS7161 with single EEPROM

In order to separate the EEPROM data space, the “AD0” settings for each PS7161 are different. Four PS7161 Redrivers read EEPROM one by one with pin “Read_En_N” asserted or de-asserted. The first PS7161 “Read_En_N” default is low, and reads EEPROM. Other “Read_En_N” are all set as high and inactive in the beginning. When the first PS7161 is done, the next “Read_En_N” will be set as low and start to read EEPROM. The operation continues until the last PS7161 is complete. EEPROM capacity minimum requirement = 256B at this moment.

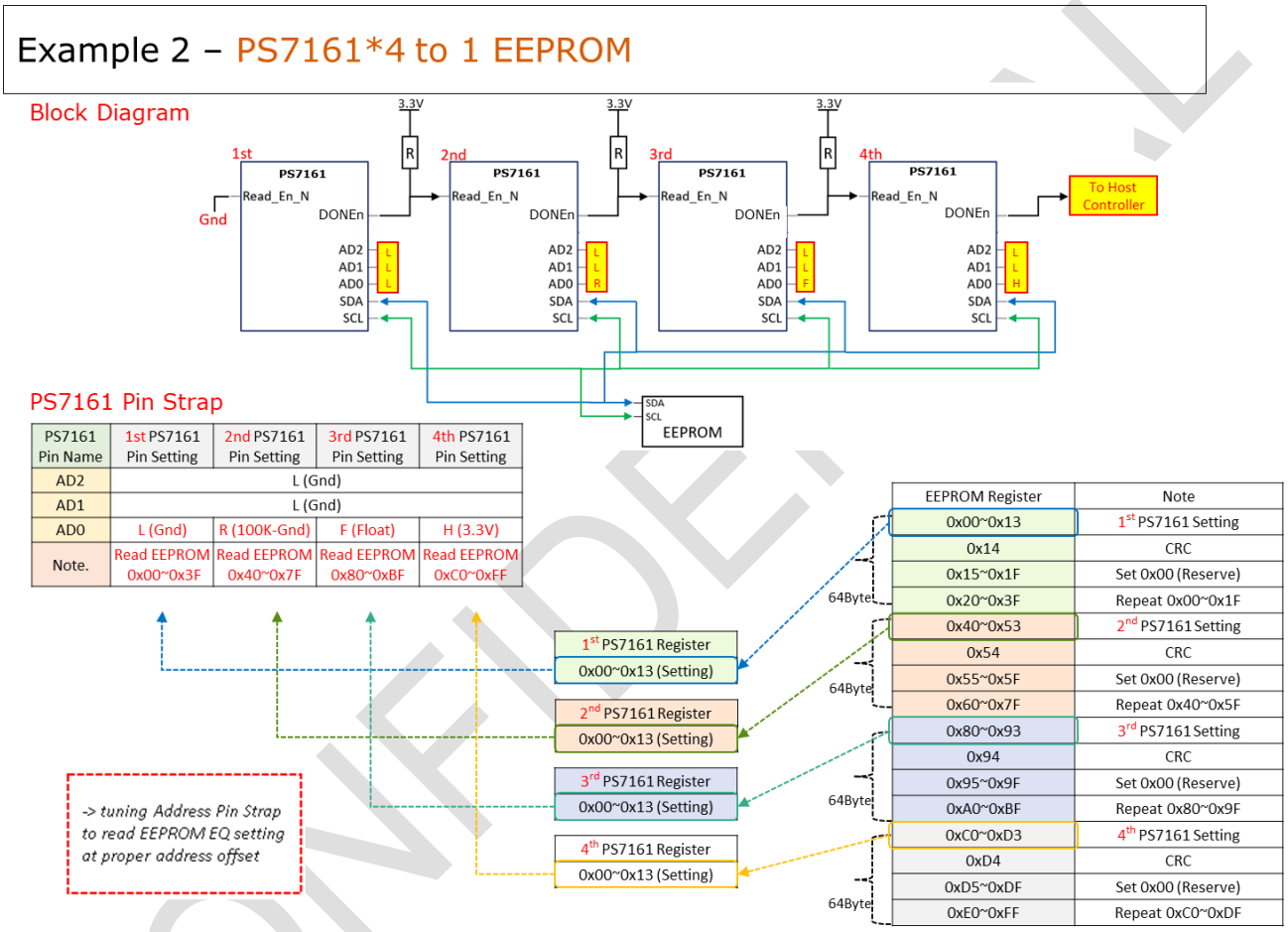
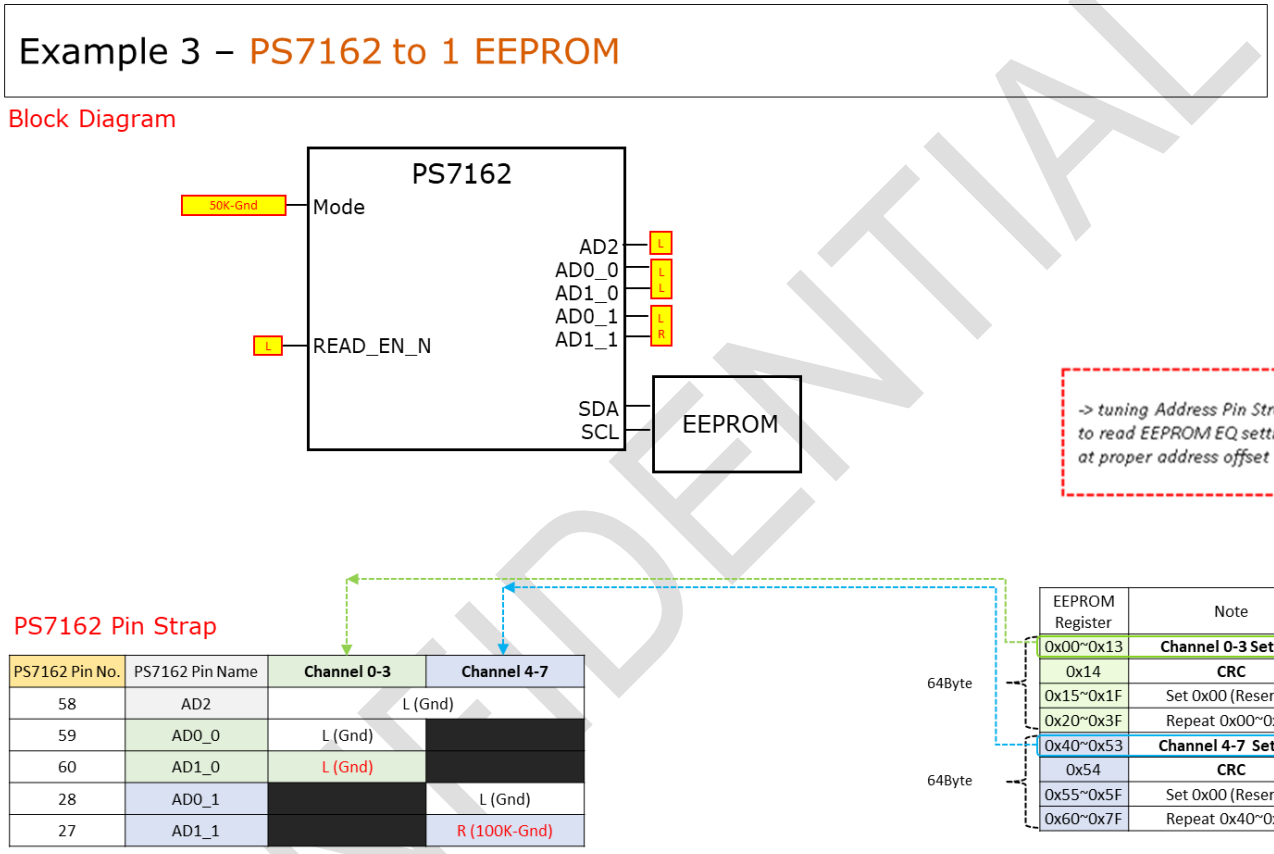


Figure 19: Four PS7161 with Single EEPROM

Example 3: Single PS7103 with single EEPROM

This case is similar to example 2. In order to separate the EEPROM data space, the “ADDR0~3” settings for each A/B side 0~7 and 8~15 channels are different. Each A/B side 0~7 and 8~15 channels respectively read EEPROM one by one with pin “Read_En_N” asserted or de-asserted. The first “Read_En_N” default is low, and reads EEPROM. Other “Read_En_N” are all set as high and inactive in the beginning. When first one is done, the next “Read_En_N” will be set as low and start to read EEPROM. The operation continues until the last PS7162 is complete. EEPROM capacity minimum requirement = 256B at this moment.



PS7162 Pin No.	PS7162 Pin Name	Channel 0-3	Channel 4-7
58	AD2	L (Gnd)	
59	AD0_0	L (Gnd)	
60	AD1_0	L (Gnd)	
28	AD0_1		L (Gnd)
27	AD1_1		R (100K-Gnd)

EEPROM Register	Note
0x00~0x13	**Channel 0-3 Setting**
0x14	**CRC**
0x15~0x1F	Set 0x00 (Reserve)
0x20~0x3F	Repeat 0x00~0x1F
0x40~0x53	**Channel 4-7 Setting**
0x54	**CRC**
0x55~0x5F	Set 0x00 (Reserve)
0x60~0x7F	Repeat 0x40~0x5F

Figure 20: Single PS7162 with Single EEPROM

6. INTEGRATION GUIDES

6.1 Power Supply

Follow the general guidelines below when designing the power supply.

- The power supply characteristics must be designed to fit the conditions outlined in the Recommended Operating Conditions in terms of DC voltage and the start-up ramp time.
- The PS7161 does not require any special power supply filter, if AC noise meets VCC_min condition. Typical local decoupling capacitors consist of a 0.1uF, one 1uF per device and must be connected as close to the VDD balls as possible. Larger decoupling capacitors that have a power bus are recommended for delivering to one or more PS7161 devices.

6.2 Layout Design Guide

Follow the guidelines below when designing the PCB layout.

6.2.1 PCB Trace

Table 27 and Table 28 are the layout guidelines for a PCB trace.

Table 27: Layout Design Guideline for PCB Trace - Part1

Net Name	Reference Plane	Differential Impedance (Ω)	Intra-Pair Skew (mil)	Inter-Pair Skew (mil)	Via Stub (mil)
TXP/TXN	GND	85+/-10%	≤ 2.5	≤ 300	≤ 10
RXP/RXN	GND	85+/-10%	≤ 2.5	≤ 300	≤ 10
CLKP/CLKN	GND	85+/-10%	≤ 2.5	N/A	N/A
	See Notes-1	See Notes-2	See Notes-3	See Notes-4	See VIA Guide

Table 28: Layout Design Guideline for PCB Trace - Part2

Net Name	Spacing to TX (mil)	Spacing to RX (mil)	Spacing to GND (mil)	Spacing to GND Reference Plane Edge (mil)	Spacing to Other Signals (mil)
TXP/TXN	S1 ≥ 9H (Microstrip < 500) S1 ≥ 12H (1000 ≥Microstrip> 500) S1 ≥ 14H (2000 ≥Microstrip> 1000) S1 ≥ 15H (Microstrip> 2000) S1 ≥ 4H (Stripline)	S2 ≥ 12H	S3 ≥ 4H	S4 ≥ 3H	S5 ≥ 5H
RXP/RXN	S2 ≥ 12H	S1 ≥ 9H (Microstrip < 500) S1 ≥ 12H (1000 ≥ Microstrip > 500) S1 ≥ 14H	S3 ≥ 4H	S4 ≥ 3H	S5 ≥ 5H

		(2000 ≥Microstrip> 1000) S1 ≥ 15H (Microstrip> 2000) S1 ≥ 4H (Stripline)			
CLKP/CLKN	≥ 5H (Microstrip) ≥ 3.5H (Stripline)	≥ 5H (MSL) ≥ 3.5H (SL)	S3 ≥ 4H	S4 ≥ 3H	S5 ≥ 5H
	See Notes-6	See Notes-6	See Notes-7	See Notse-8	See Notes-9

Notes

1: Keep the GND reference plane of TX/RX/CLK traces complete.
2: Keep the impedance of TRACE the same in every layer.
3: Keep the intra-pair skew as small as possible.
4: “Inter-Pair Skew” means the skew between each TX lane or the skew between each RX lane. It is not necessary to make the skew between a TX lane and a RX lane within 300mil.
5: The total length should be as short as possible.
6: “H” is the distance between TRACE and its closest reference plane. The spacing should be as large as possible.

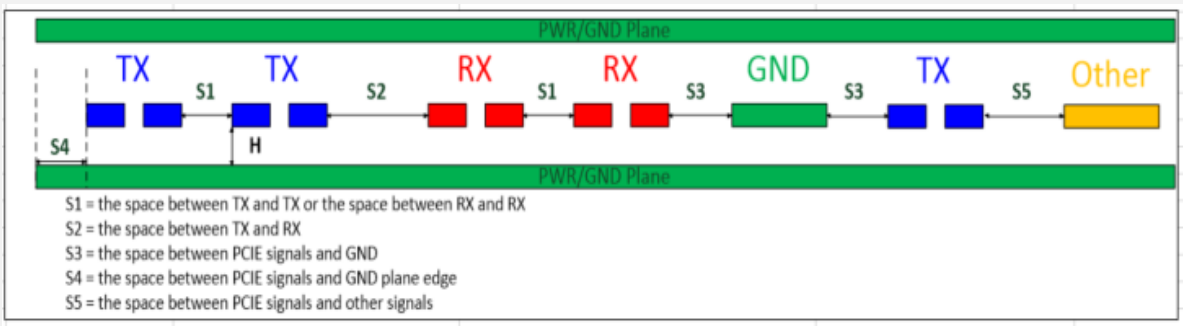
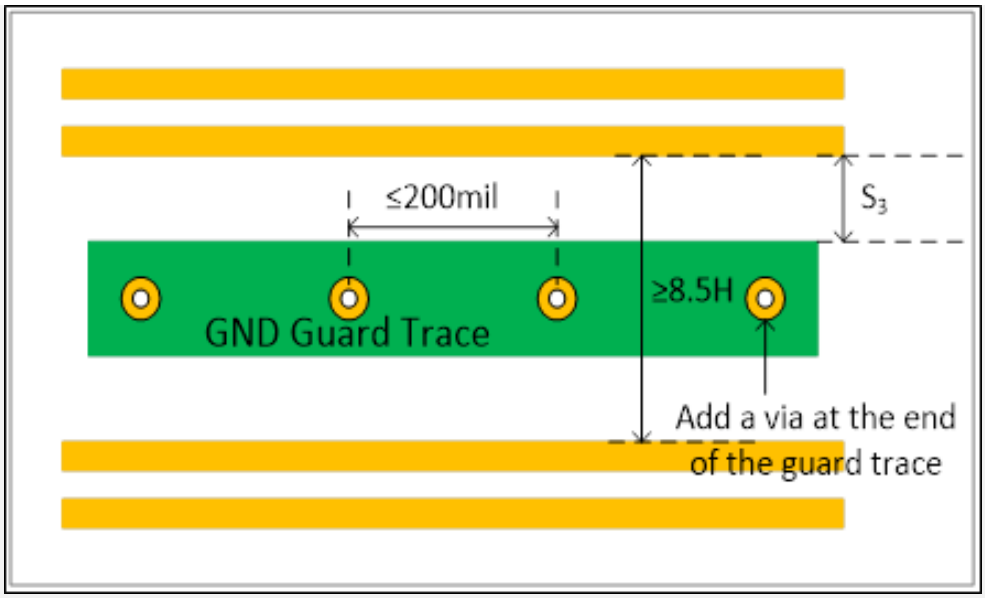


Figure 21: The reference of PWR/GND Plane

7: Keep the spacing to GND larger than 4H.
8: The space between signal and GND plane edge should be large enough to keep the return current path complete.
9: The other pair/signal includes TRACEs of other interfaces, such as SDRAM, NAND, POWER…etc. Keep the spacing of those TRACEs larger than 5H.
10: It is preferred to add GND guard traces (planes) between TX/RX signals to enhance their isolation.
11: If the spacing between TX/RX signals already meets S2≥12H, it is not necessary to add GND guard traces.
12: If there are GND guard traces between TX/RX signals, place GND vias along the guard trace and the distance between vias should be smaller than 200mil.
13: If there are GND guard traces between TX/RX signals and S3≥4H is difficult to meet, S3≥3H is acceptable. But make sure the spacing between TX/RX signals is larger than 8.5H as in the following figure.



14: Keep the spacing of via to trace larger than 8H.

15: Place GND trace between trace and via.

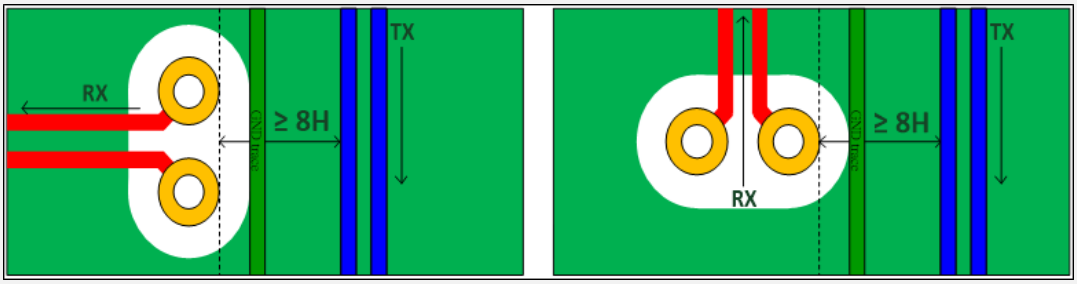


Figure 22: The reference of GND trace

6.2.2 Finger

1. The plane under edge-fingers needs to be voided in order to reduce the capacitance of those fingers. The recommended void area for different form factors is listed below. Note that certain inner layers are not removed.

Table 29: Layout Design Guideline for Add-In Card Form Factor

Form Factor	Suggestion
Add-In Card	Keep one inner layer (Figure 23)

For the **Add-In Card Form Factor**, the recommended void area under edge-fingers is shown in Figure 23. Two inner plane layers are kept to reduce the crosstalk between TX and RX, while other inner plane layers are voided. The distance between RX fingers and the inner plane should be at least 0.52mm. The distance between TX fingers and the inner plane should be at least 0.52mm. If there is no available inner plane layer laying at least 0.52mm above bottom edge-fingers, the inner plane area may need to be fine-tuned (vias are neglected to show GND planes clearly)

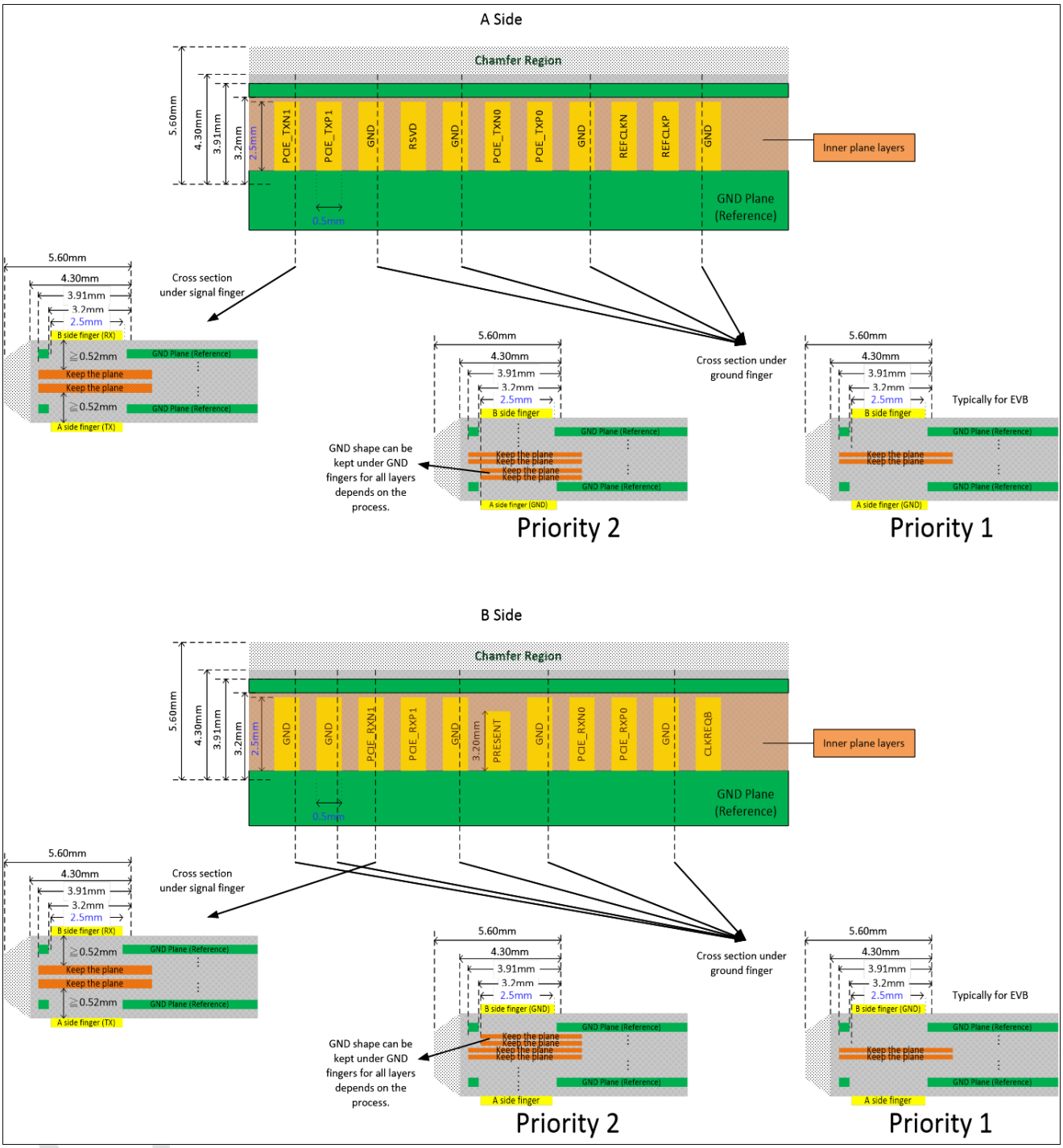


Figure 23: The Reference Layout for AIC Form Factor

2. **Add-in Card** GND vias position

Vertical position of GND vias: place the GND vias close to Add-in Card edge-fingers in order to reduce the inductance of the ground connection (within 6 mil).

Horizontal position of GND vias: the GND via horizontal positions should follow Figure 24; connect the GND finger to the GND via with a trace whose width is equal to or larger than the diameter of the via pad. Note that traces of REFCLKP and REFCLKN should avoid the GND via between them.

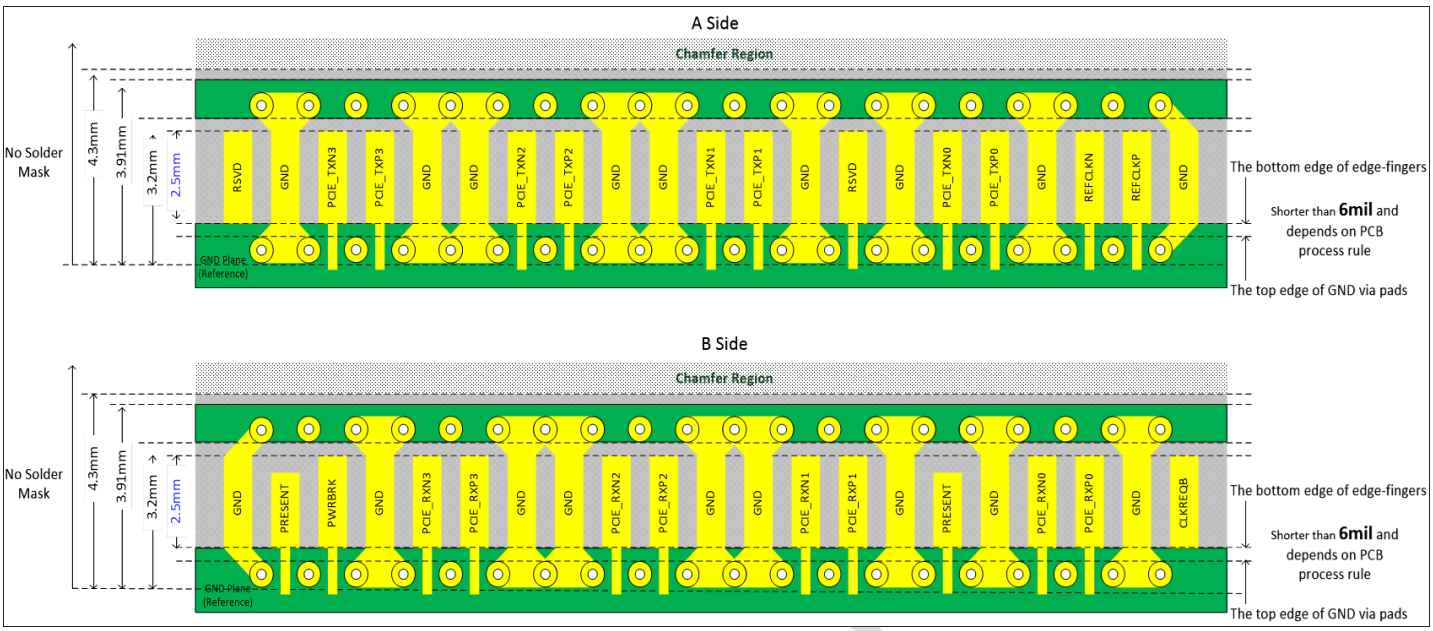


Figure 24: The Reference Layout for GND-Vias

3. The length of **Add-in Card** edge-fingers is 2.5 mm. There is a 1.3 mm gap between the edge-fingers and the chamfer region is shown in Figure 25: The Gap Between Edge-Fingers and Chamfer Region

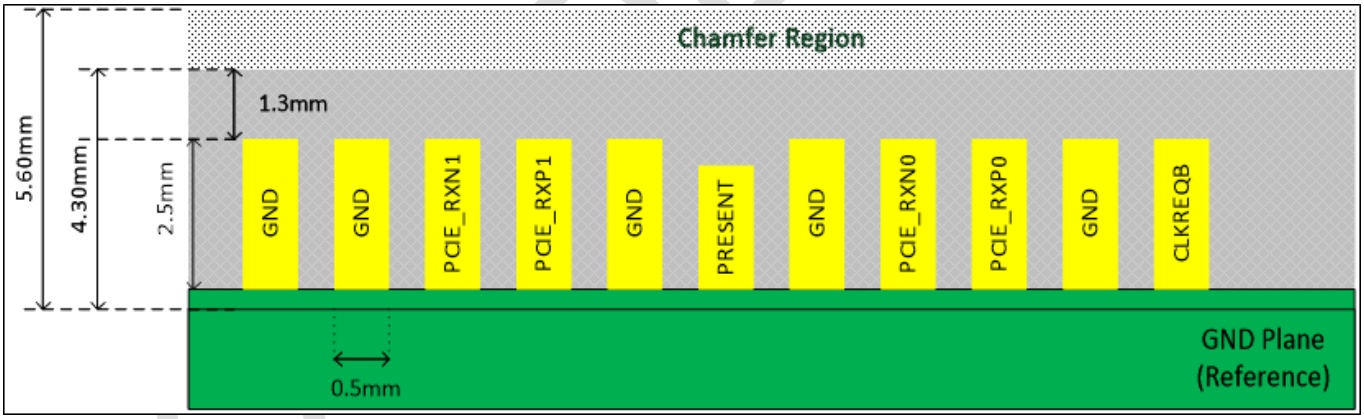


Figure 25: The Gap Between Edge-Fingers and Chamfer Region

4. The following auxiliary pins on **Add-in Card** must be terminated in order to reduce the crosstalk between adjacent high-speed TX/RX pairs.

(1)A19--RSVD, (2)A32--RSVD, (3)B12--CLKREQ#, (4)B17--PRSNT2#, (5)B30--PWRBRK#, (6)B31--PRSNT2#

The recommended DC blocking capacitor is 1.0pF+/-10% and the recommended resister is about 42.5ohm +/-10%.

The trace length from the edge-finger and to the termination circuit should be as short as possible or be shorter than 500mil.

Figure 26: The Reference Layout for A-side

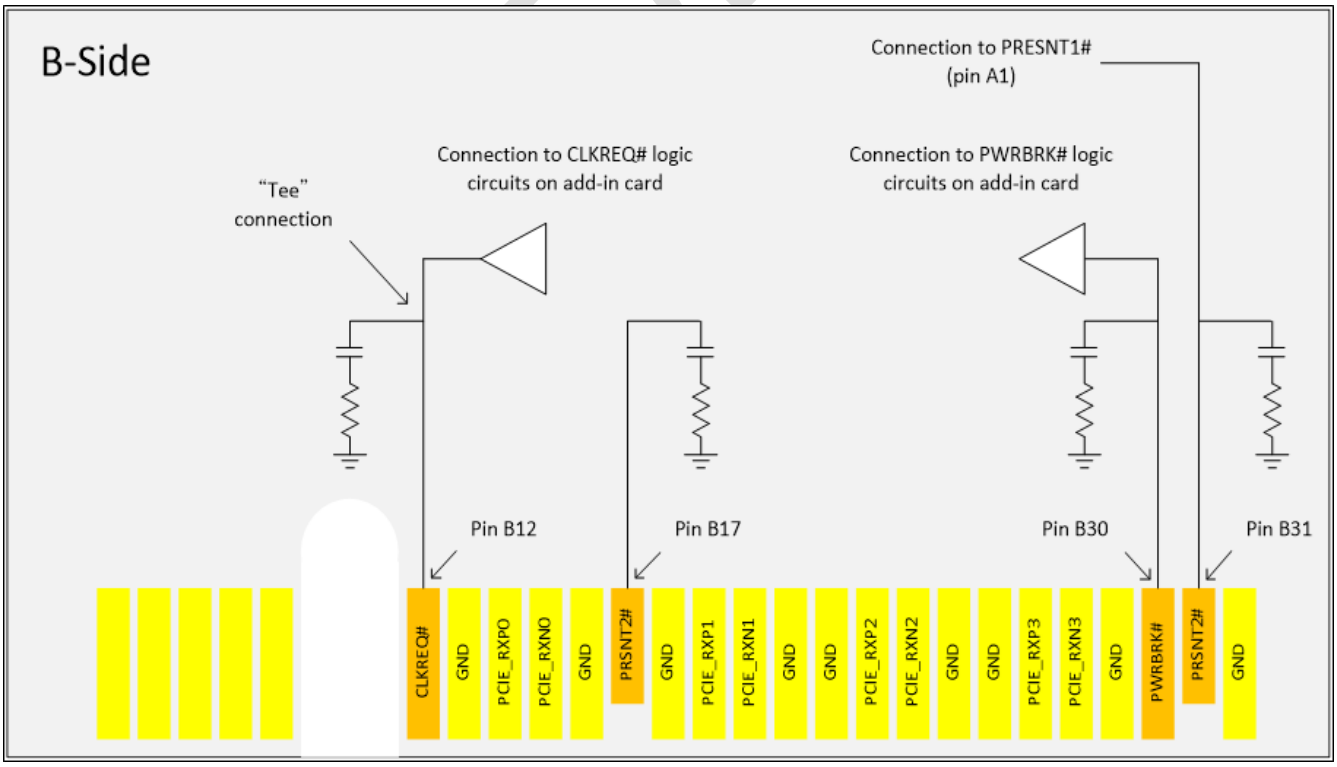
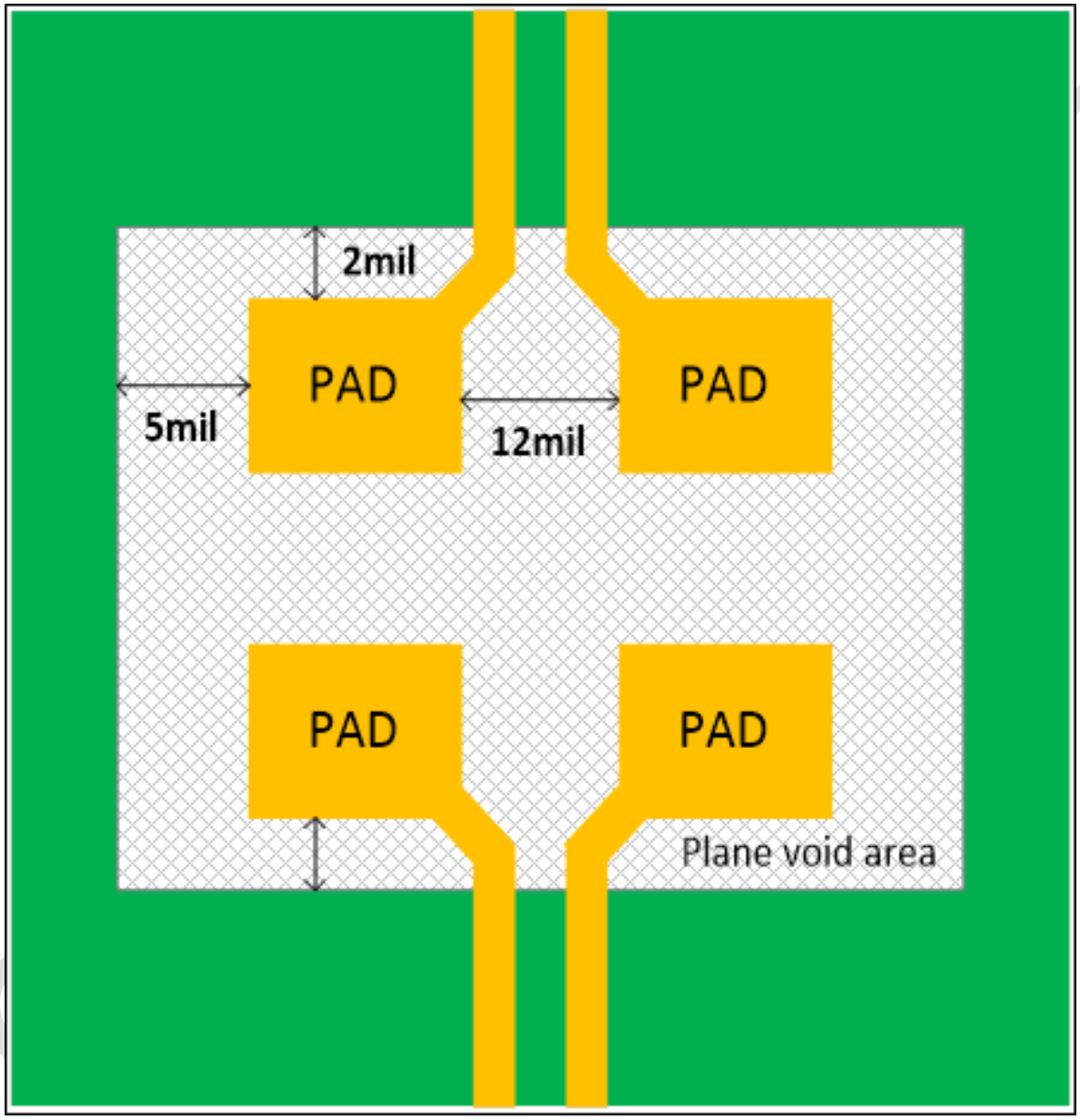


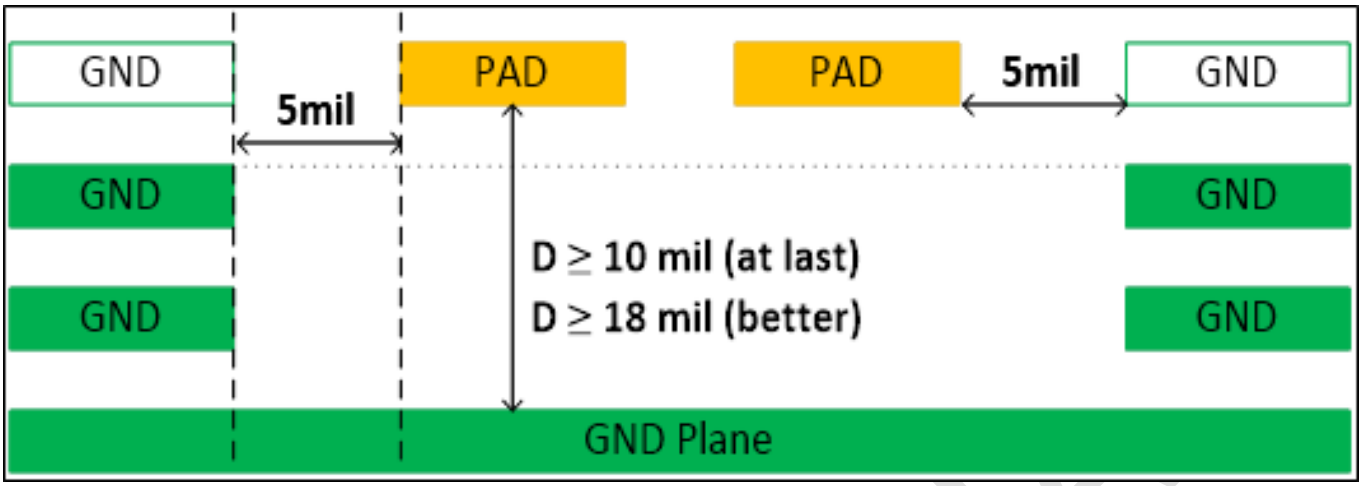
Figure 27: The Reference Layout for B-side

6.2.3 AC-Coupling Capacitor

1. Place AC coupling capacitors close to edge-fingers. The trace length from the capacitor to the edge-finger should not exceed 450mil.
2. Use small AC coupling capacitor sizes, such as 0201. 220nF is recommended.
3. It is recommend to void plane beneath ac coupling capacitors as shown in Figure 28.



(a)



(b)

Figure 28: The Reference Layout for AC-Coupling Capacitors Option 1 (a) Top View (b) Sectional View

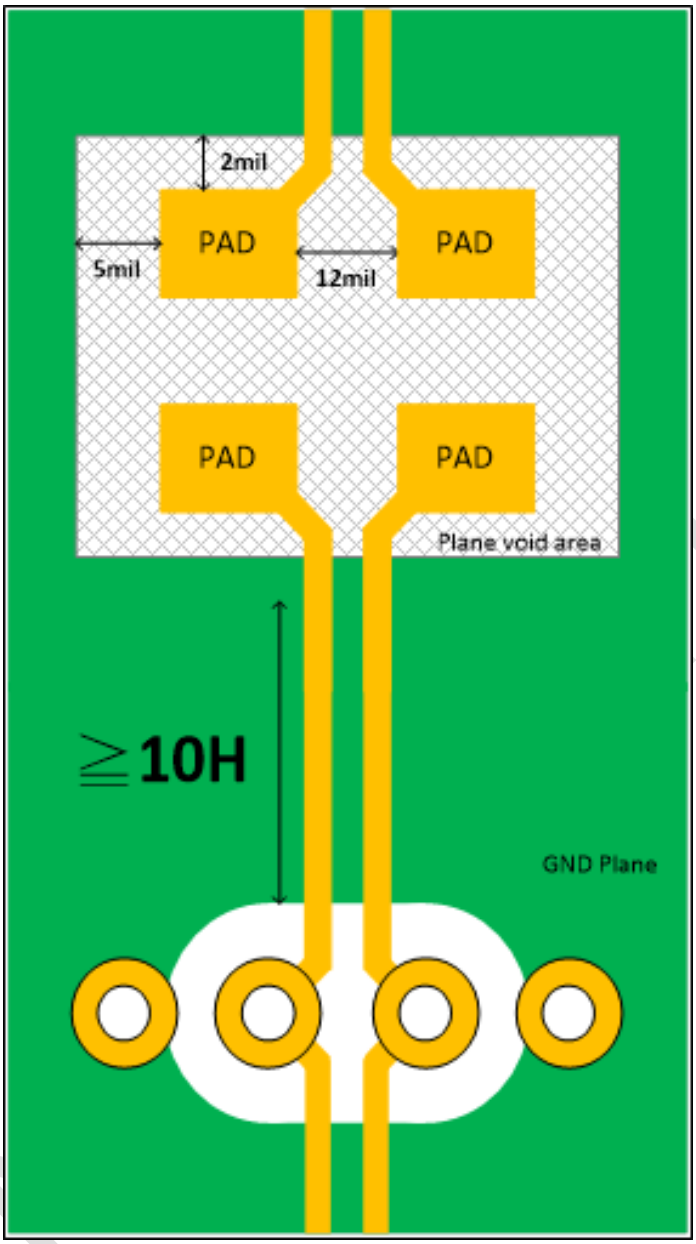


Figure 29: The Reference Layout for AC-Coupling Capacitors Option 2 Top View and Sectional View

4. Keep the distance between the closest via anti-pad from void at least 10H.
5. Based on different stack up, the GND void may need to be fine-tuned to match the impedance of TRACE.

6.2.4 VIA

1. For the first priority, there should be no via on TX/RX/CLK TRACE. If via can't be avoided, the number of via on TX/RX/CLK TRACE should be minimized.

2. Remove non-functional pads from internal layers to minimize excess via capacitance.

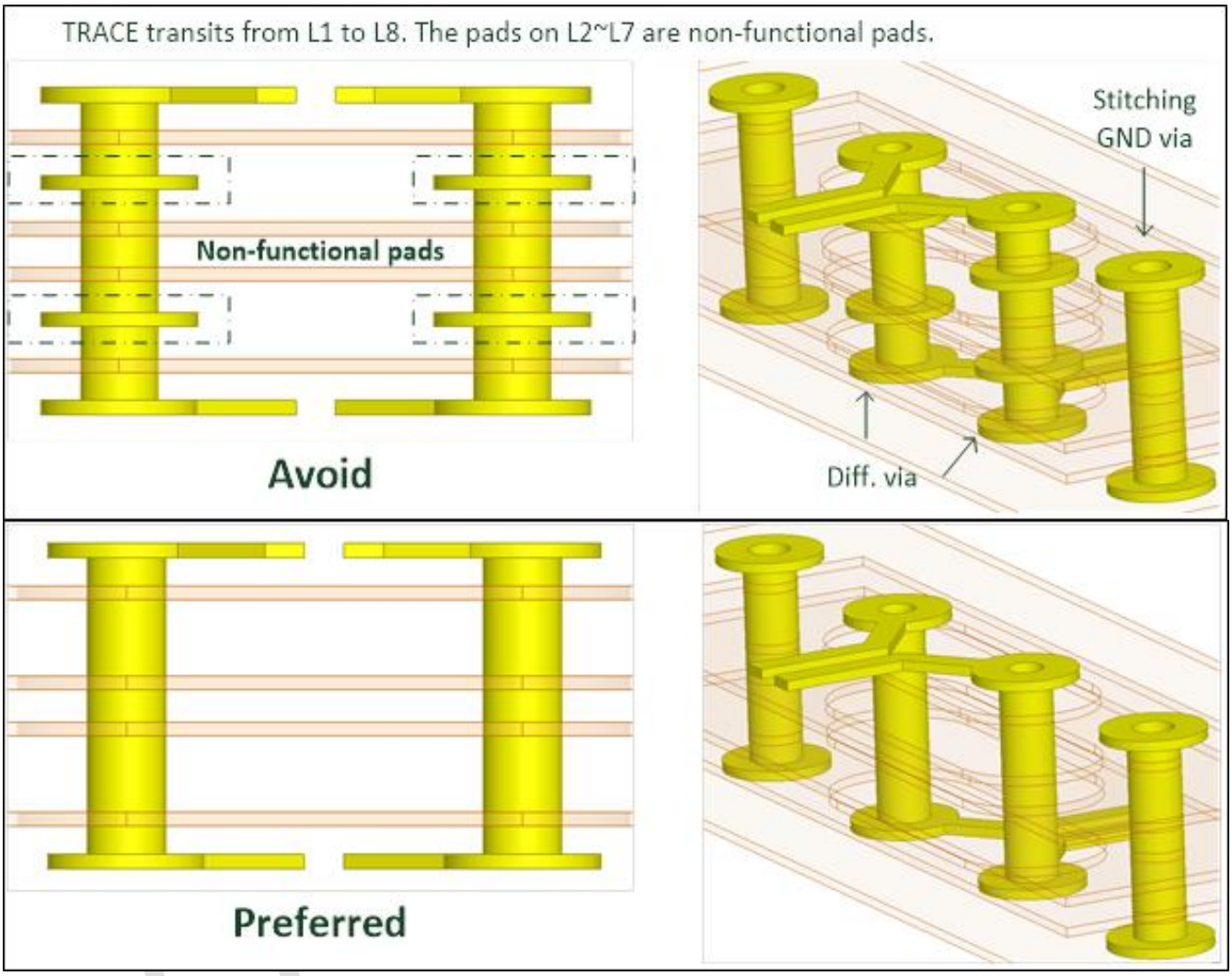


Figure 30: Remove Non-Functional Pads

3. Keep VIA stub as short as possible. For PTH process, VIA stub is shorter if TRACE transits from top-layer to bottom-layer, compared with top-layer to L3. VIA stub can be removed by using 1) top-layer to bottom-layer routing 2) backdrill 3) HDI process as shown in Figure 31.

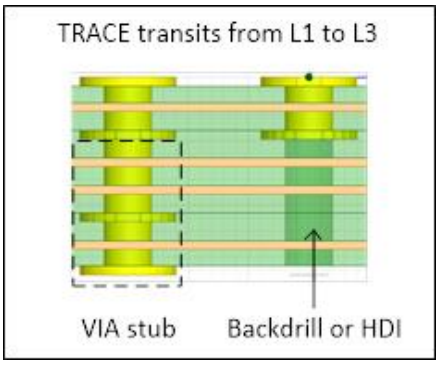


Figure 31: The Back-Drill and HDI Method

4. When TRACE transits to another layer, add stitching VIAs symmetrically and close to signal VIAs in order to avoid reference plane discontinuity. If the reference plane is the same after layer transition, it is not necessary to add stitching VIAs. For example, TRACE transits from L1 to L3. The reference plane is still L2. Figure 32 shows that the signal transits from L1 to L4 and the stitching GND via connects L2 and L5.

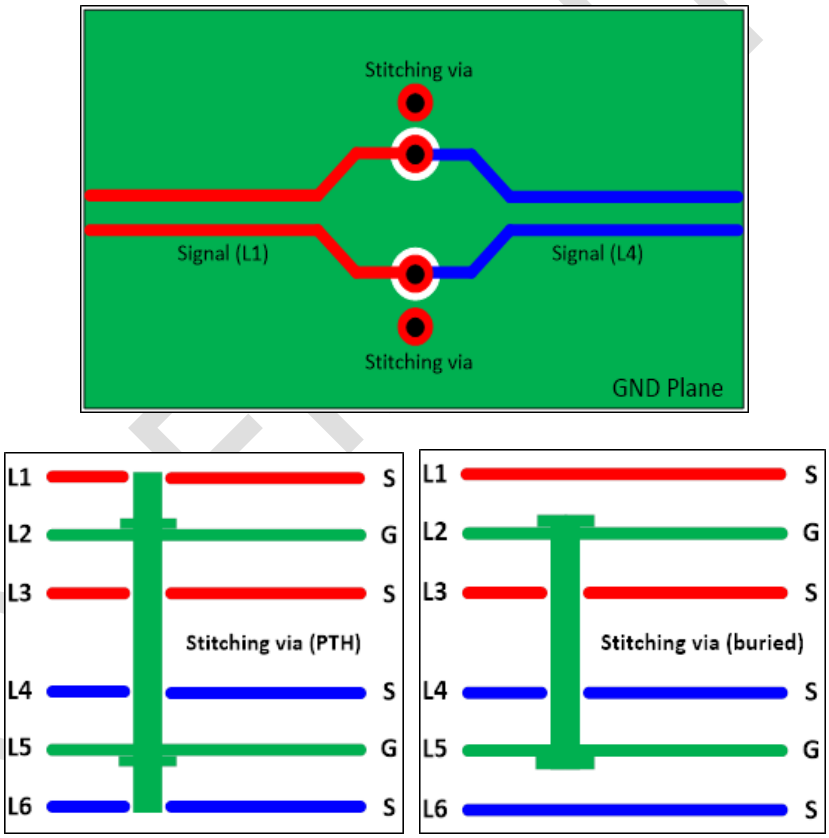


Figure 32: The Reference Layout for Stitching Vias

5. For plated through hole process, it is recommended to use the following differential via pattern to optimize the impedance as shown in Figure 33 and Table 30.

- Note that the diameter D1 is referred to the diameter before plating.
- Anti-pad radius of the top and the bottom layer can be larger than S3.

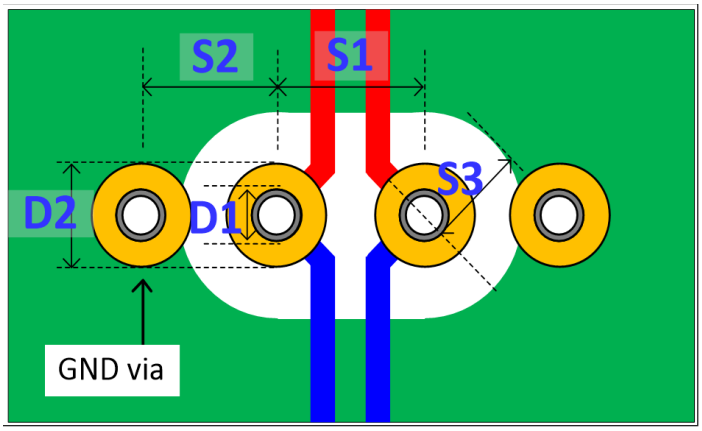


Figure 33: The Reference Layout of Differential Via Pattern for PTH Process

Table 30: Diameter Table of Differential Via Pattern

	Phison EVB Pattern 1	Pattern 2	Pattern 3
D1	8 mil	10 mil	4 mil
D2	16 mil	16 mil	10/12 mil
S1	25 mil	30 mil	23 mil
S2	20 mil	25 mil	20 mil
S3	14 mil	15 mil	10 mil

6. For HDI process, GND or PWR plane under via pads should be voided. Depending on the stack-up, at least the closest plane beneath via pads need to be voided as shown in Figure 34.

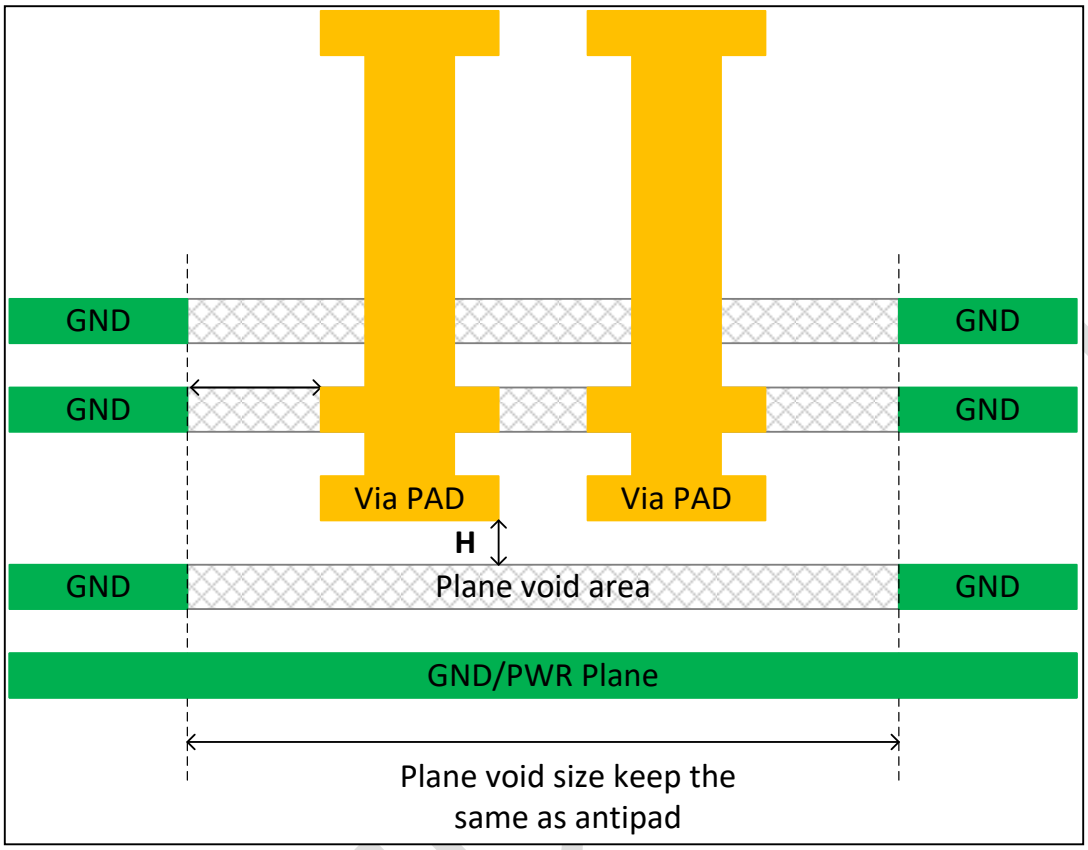


Figure 34: The Reference Layout of GND/PWR Plane for HDI Process

7. In the HDI process, stacked via is preferred over stagger via as shown in Figure 35.

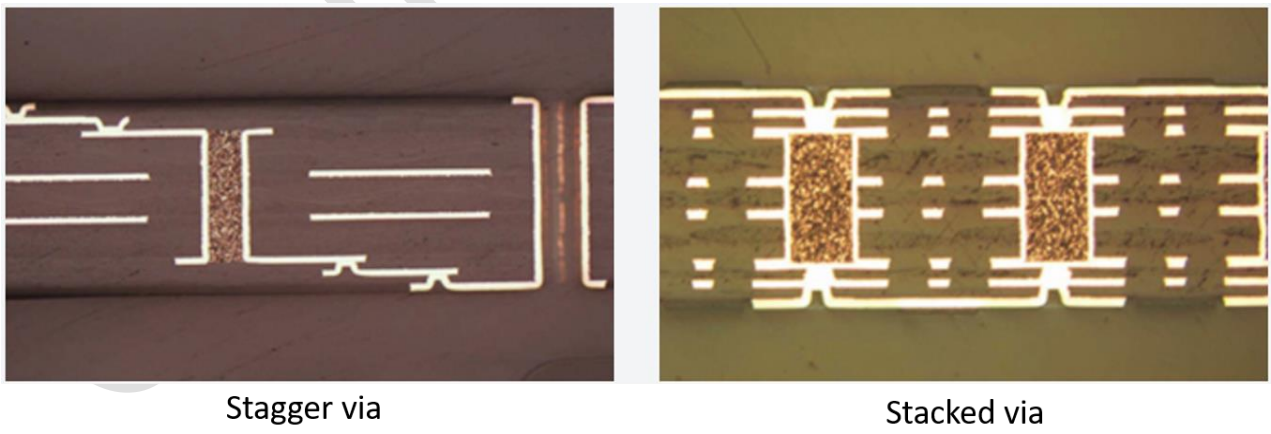


Figure 35: Comparison Between Stagger Via and Stacked Via

8. For different stack-ups, the via pattern may be fine-tuned to match the impedance of TRACE.

6.2.5 General Design

1. Proceed the length matching close to where the length mismatch occurs, and use the back-jog routing rather than the serpentine routing, as shown in Figure 36.

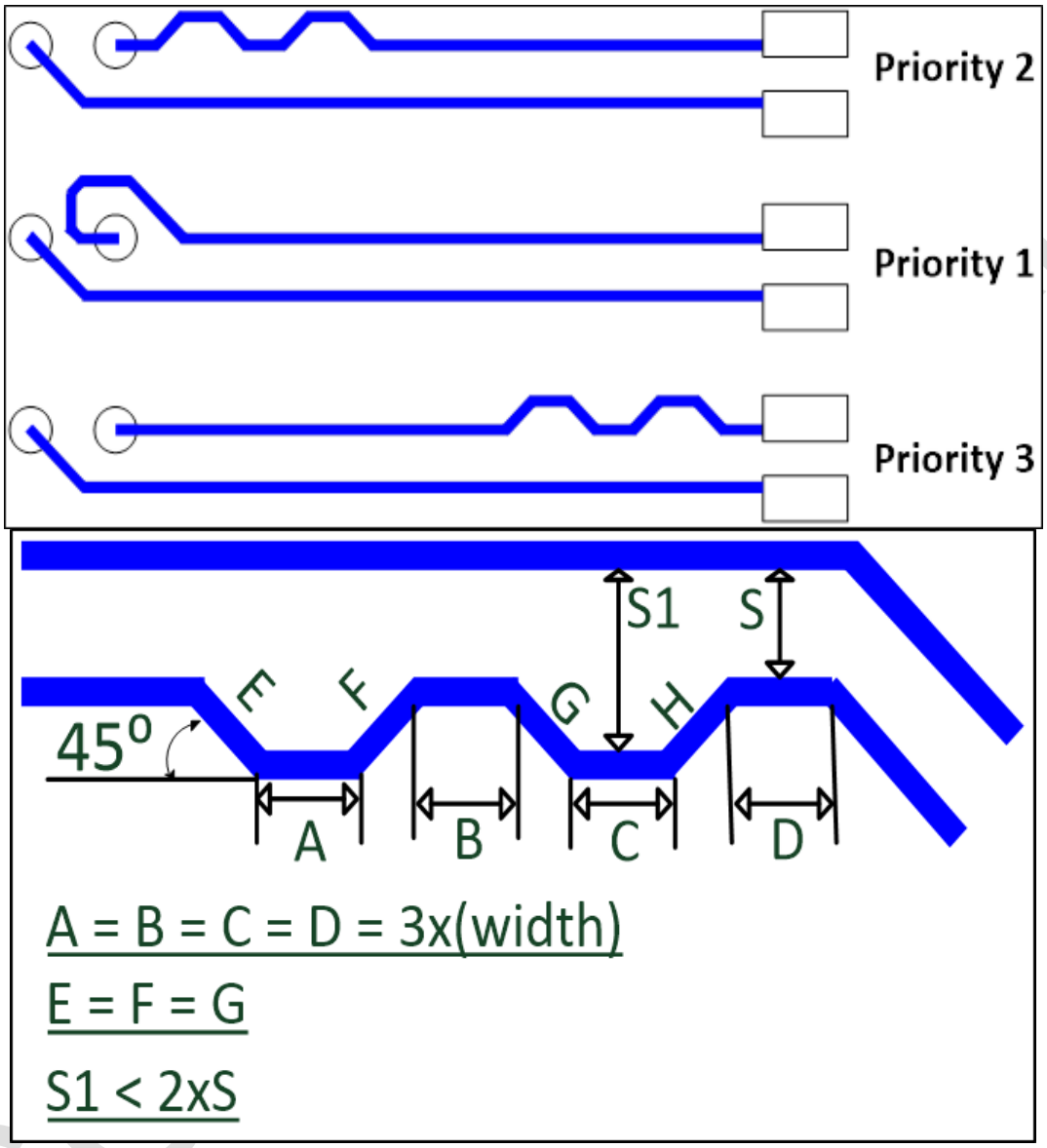


Figure 36: Method of TRACE Length Mismatch

2. Do not count the trace length inside FINGER-PAD, as shown in Figure 37.

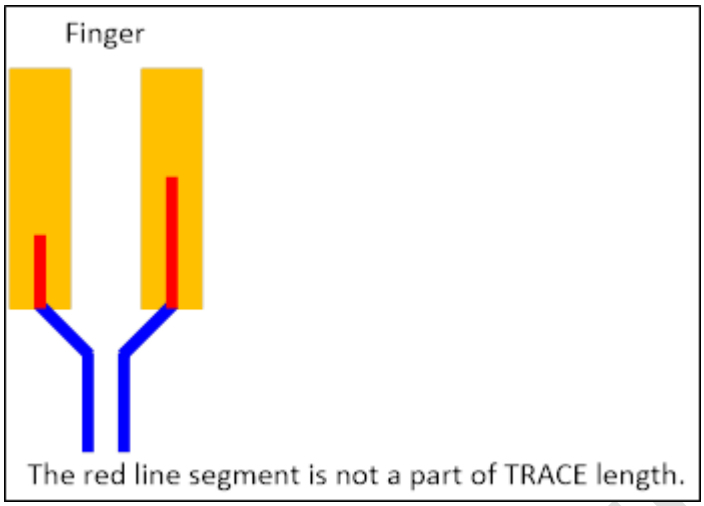


Figure 37: The Count Method of TRACE Length

3. Use the symmetrical routing for TRACE/VIA/FINGER-PAD/CAPACITOR-PAD.

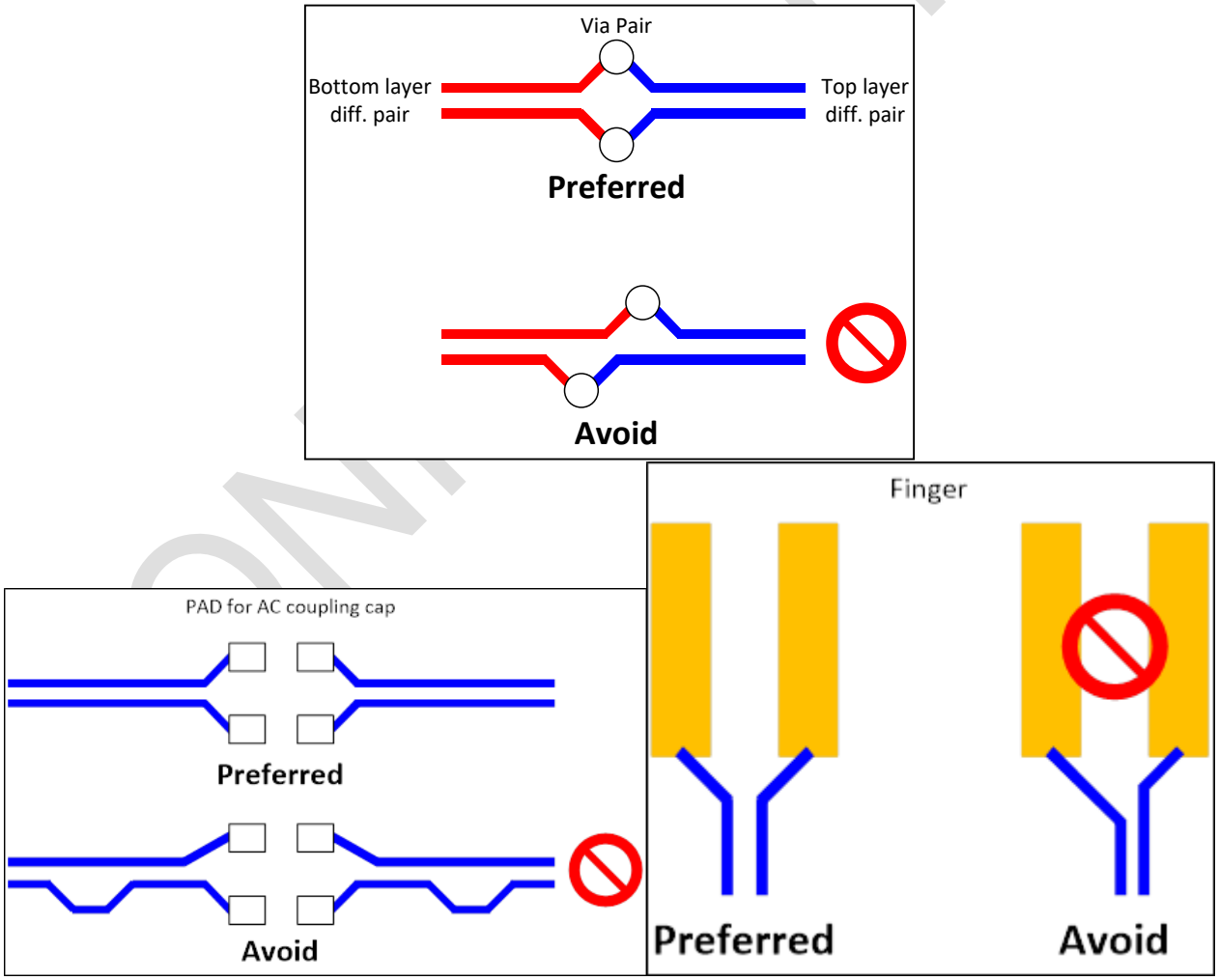


Figure 38: The Reference Layout of Symmetric Routing

4. GND void under ball pad is required, but RX under TX shall be avoided. Void one closest plane beneath ball pad.

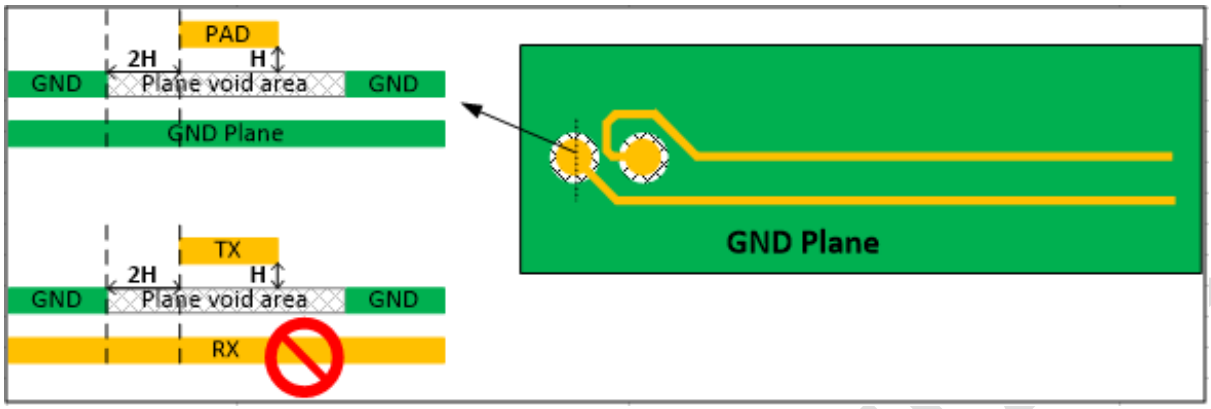


Figure 39: The Reference Layout of Ball Pad Method

5. Minimize the number of bends. If bends are required, the bend angle should be greater than 135 degrees.

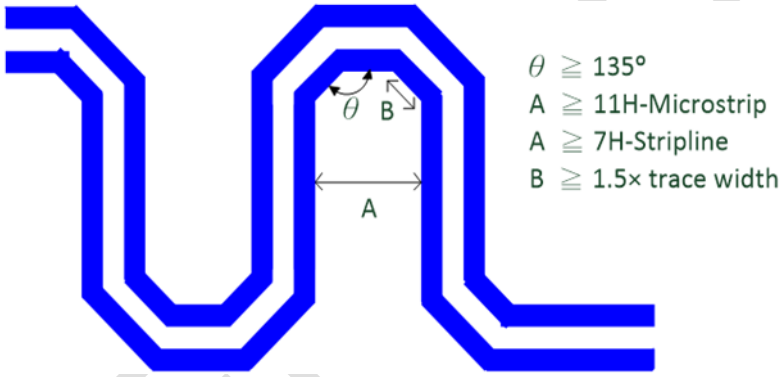


Figure 40: The Reference Layout of the Bended Traces

6. Non-interleave routing (RX group in the same layer, TX group in another layer) is preferred.

7. Stripline is preferred. For dual stripline, avoid trace overlaps when TRACEs are routed on the adjacent layer.

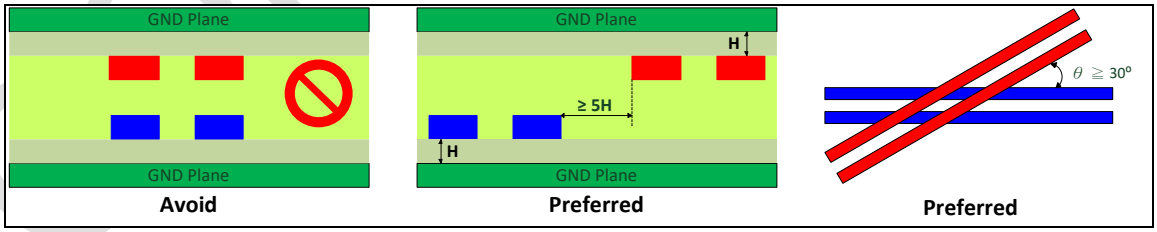


Figure 41: The Reference Layout for Dual Stripline Routed on Adjacent Layer

8. Do not place test-pads on high-speed TX/RX signals.

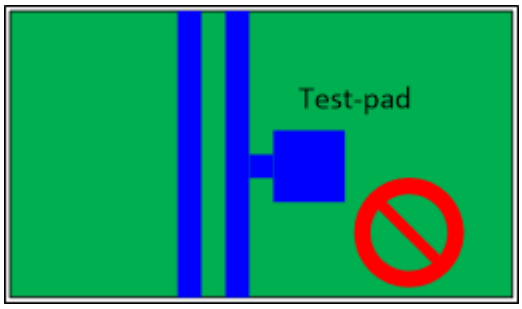


Figure 42: The Reference Layout of Test-pad

9. Arc is more preferred in the corner than the 45-degree angle.
10. For two rows mounted connector footprint, the recommended void area under edge-pad is shown in Figure 43.

    The GND void may be fine-tuned to match the impedance of TRACE based on different stack-up.

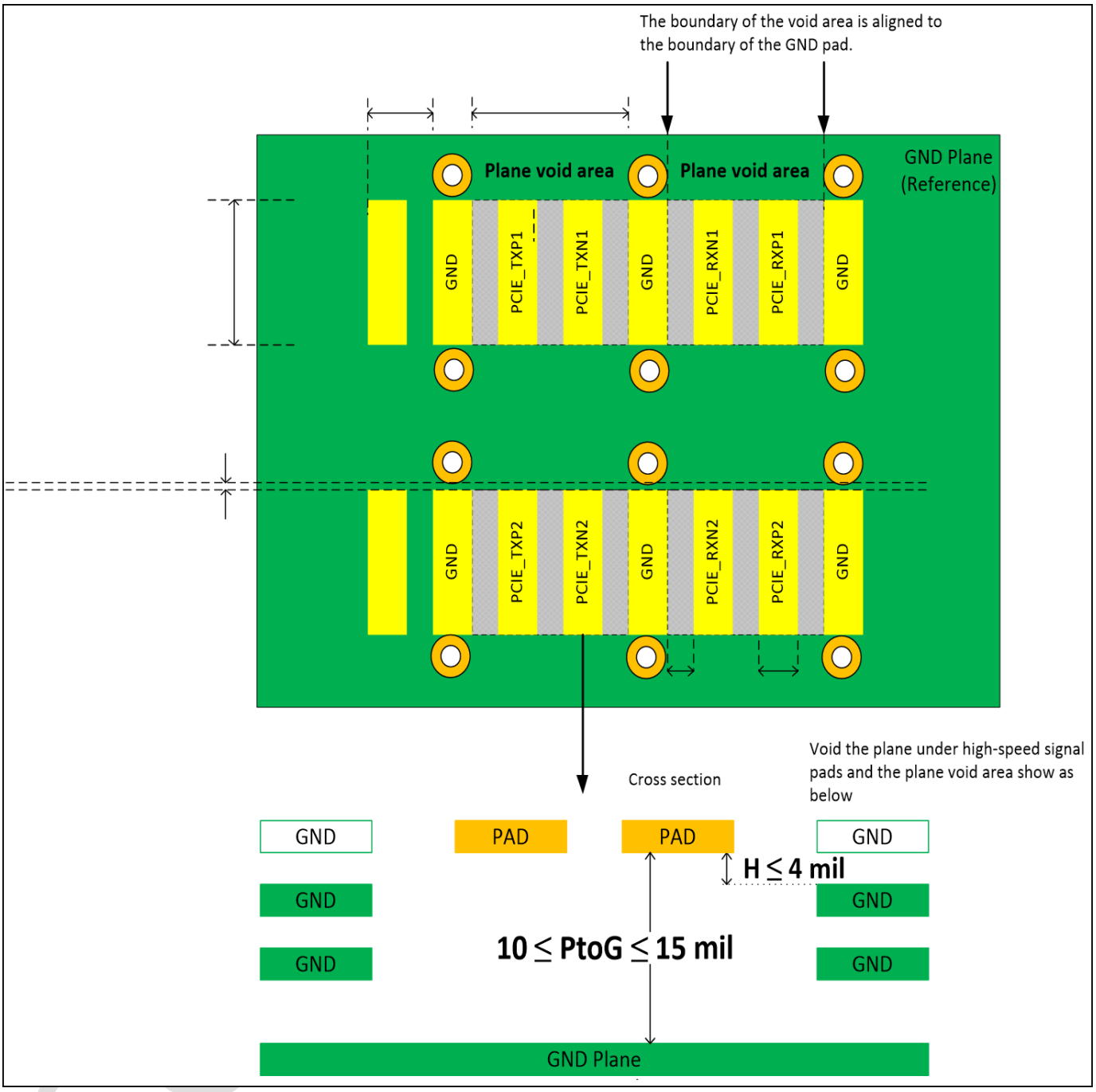


Figure 43: Two Rows Mounted Connector Footprint

The recommended signal path is shown in Figure 44.

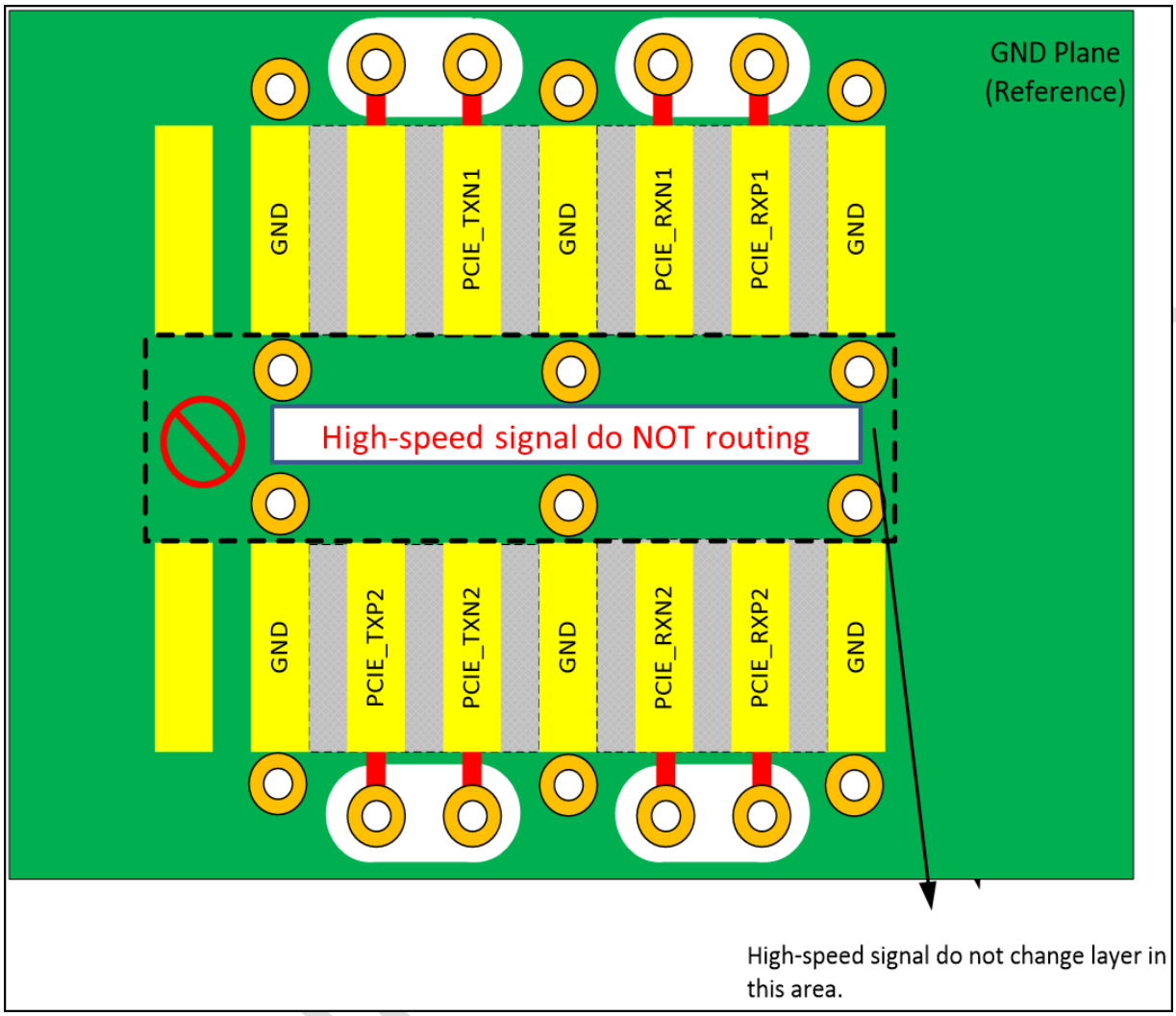


Figure 44: Recommended Signal Path

11. For one row mounted connector footprint, the recommended void area under edge-pad is shown in 錯誤! 找不到參照來源。.

    The GND void may be fine-tuned to match the impedance of TRACE based on different stack-up.

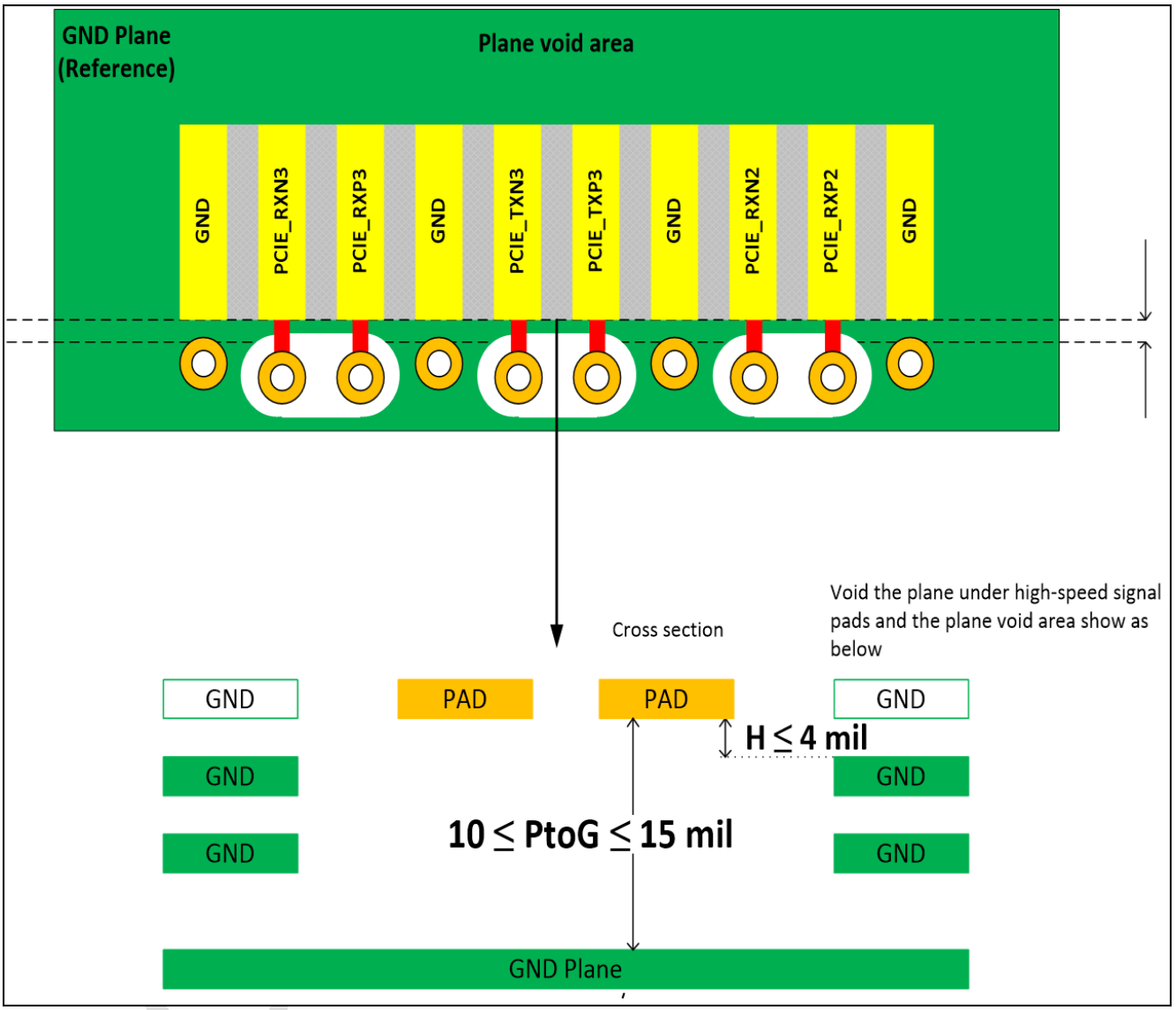


Figure 45: One Row Mounted Connector Footprint

12. The recommended routing for M.2 slot is shown in 錯誤! 找不到參照來源。.

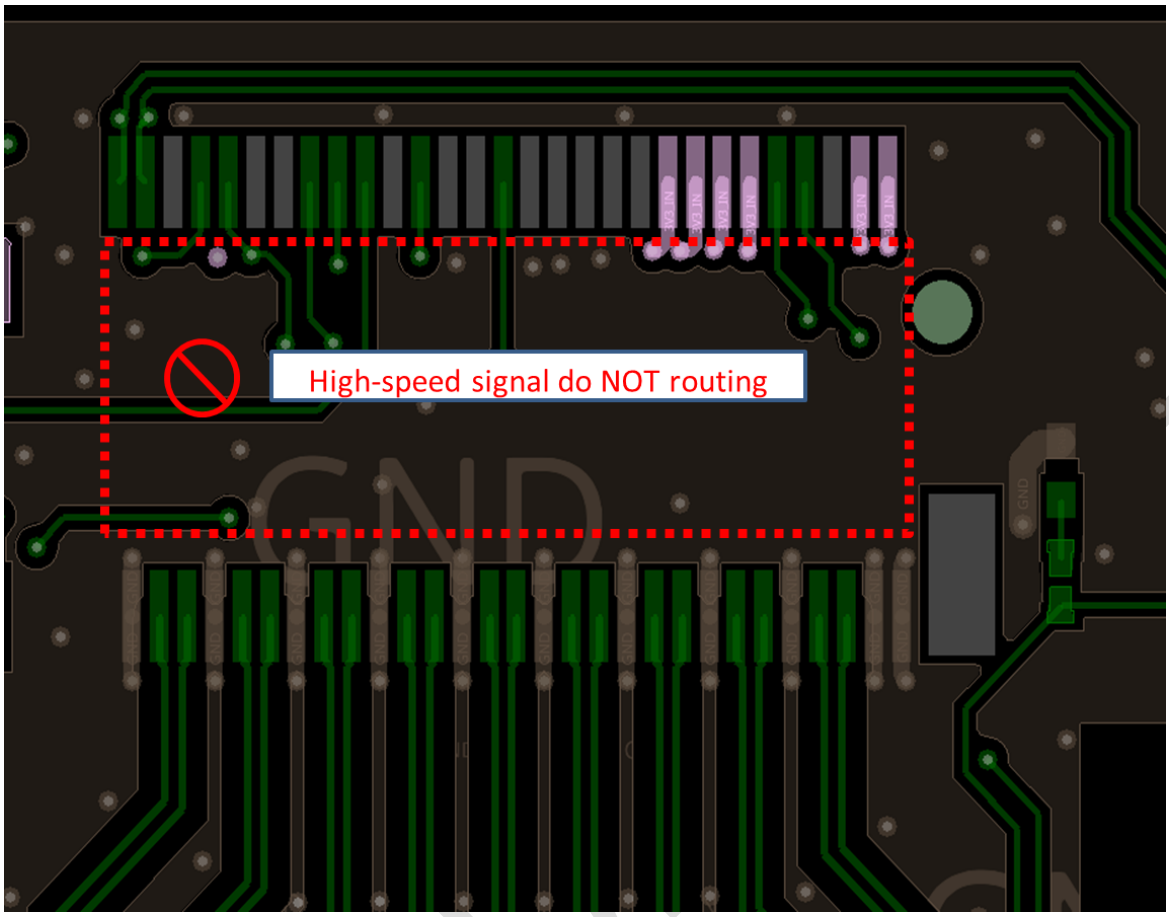


Figure 46: M.2 Slot Recommended Routing

6.2.6 Phison PCB Implementation

1. Decoupling capacitors should be placed as close as possible to power pin.

PCB TOP view:

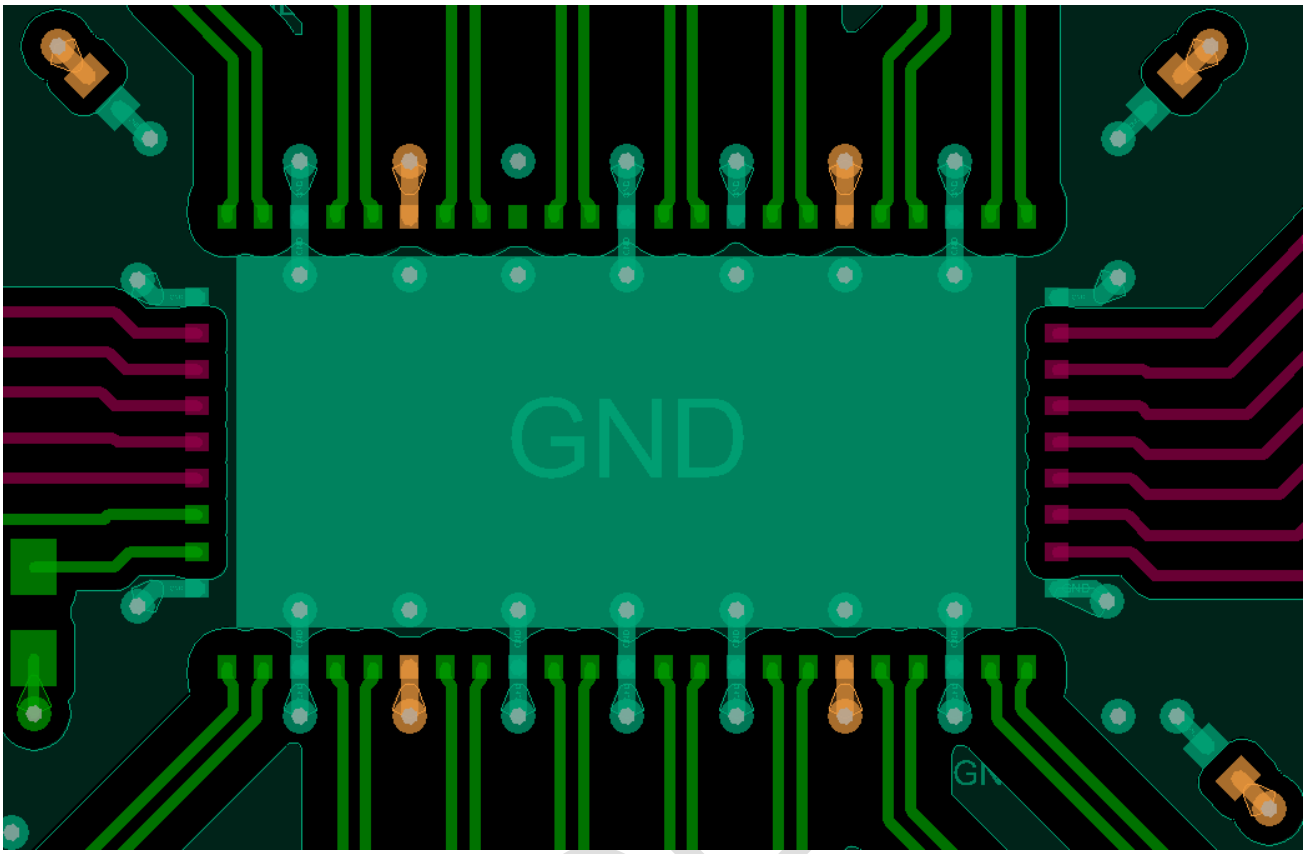


Figure 47: The Reference Layout of Decoupling Capacitors

6.3 Thermal Design Guide

The PCB is an important path to dissipate heat, especially in the case without a heatsink. The following are suggestions for increasing the heat dissipation capacity of the PCB.

6.3.1 General Rules

1. The PCB is composited by conductive and insulating layers in the form of a laminated sandwich structure. Conductive layer is a good thermal conductor. Choose a stack-up with a higher proportion of the conductor layer, the better for thermal.
2. Maximize GND/PWR plane area on the top layer especially around package area to conduct heat away from the package, and provide a larger surface area for heat to escape the PCB through convection. Maximizing the inner conductive layer cooper coverage also helps to conduct the heat away more effectively.
3. The conductive layers are connected by vias. Maximizing the number of thermal via underneath the package improves the thermal performance.

6.3.2 Thermal Characteristics

Thermal characteristics listed in Table 31 is simulated and calculated according to JEDEC test standard, and these values are environmental related. In other words, these values could vary with different boundary conditions (e.g., airflow, pcb size and pcb copper rate). Prediction of junction temperature using these values may cause error. Package thermal model is available for thermal simulation. Designers can evaluate thermal characteristics in actual applied environment.

Table 31: Thermal Resistance of PS7161

Thermal Characteristics		PS7161	UNIT	Note
$R_{\Theta JA}$	Junction-to-ambient thermal resistance	54.5	°C/W	1
$R_{\psi JT}$	Junction-to-top characterization parameter	6.8	°C/W	1
$R_{\psi JB}$	Junction-to-board characterization parameter	32.1	°C/W	1
$R_{\Theta JB}$	Junction-to-board thermal resistance	30.5	°C/W	1
$R_{\Theta JC}$	Junction-to-case thermal resistance	41.5	°C/W	1

Note:

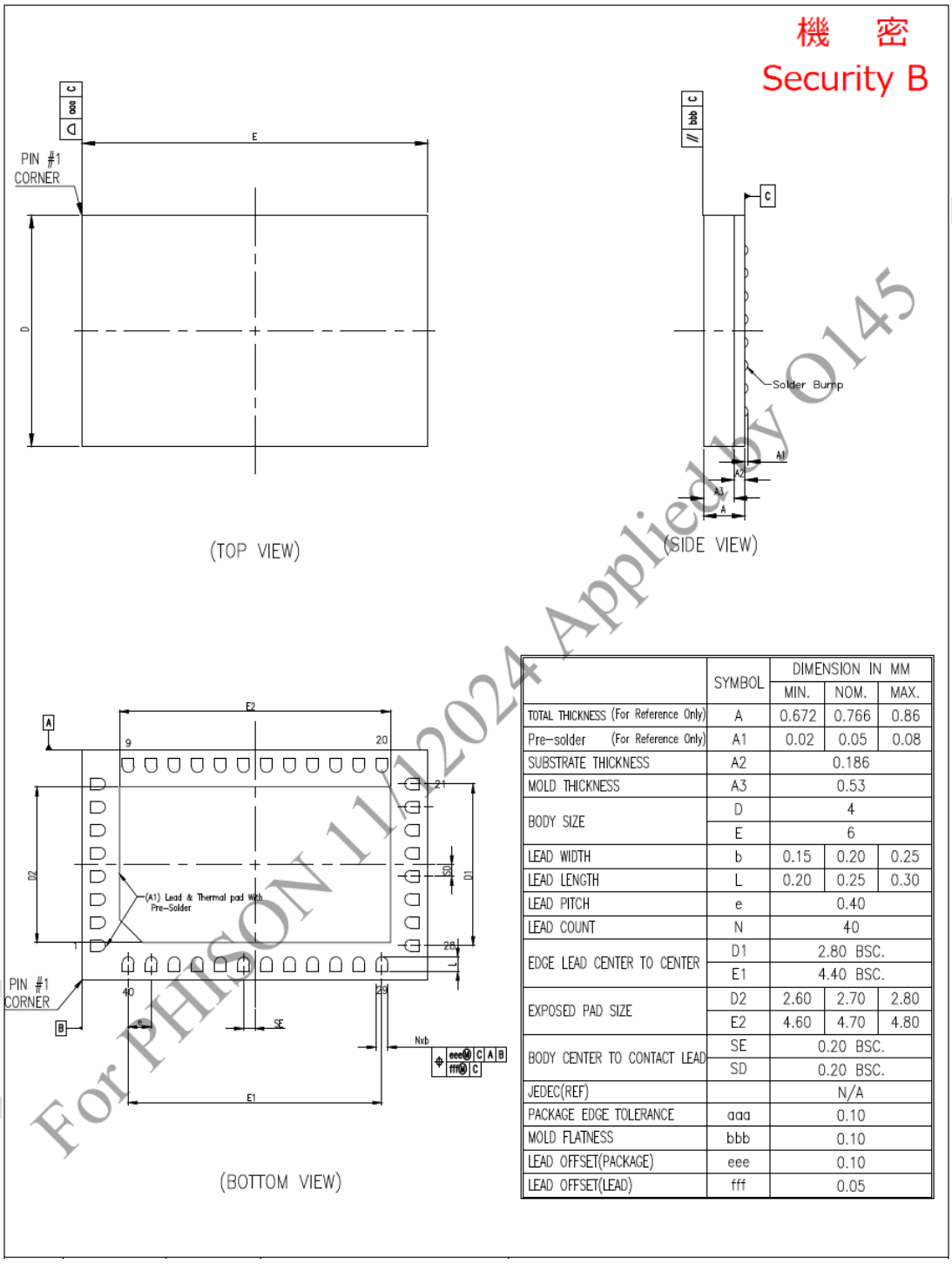
1. $R_{\Theta JA}$ = (Junction temp. - Ambient temp.)/Power dissipation. Represents thermal resistance of the heat flows from the chip to ambient air.
   $R_{\psi JT}$ = (Junction temp. - Package top center temp.)/Power dissipation
   $R_{\psi JB}$ = (Junction temp. - Board temp.)/Power dissipation
   $R_{\Theta JB}$ = (Junction temp. - Board temp.)/Power dissipation;
   $R_{\Theta JC}$ = (Junction temp. - Package top center temp.)/Power dissipation;

7. PS7161 Batch File Guides for VNA Test

If VNA is required, please contact PM to obtain the batch file and user guide.

8. OUTLINE DIMENSION

- Package: 40-Balls FCLGA (6.0 mm (x-axis) x 4 mm (y-axis) / 0.40 mm Lead Pitch)

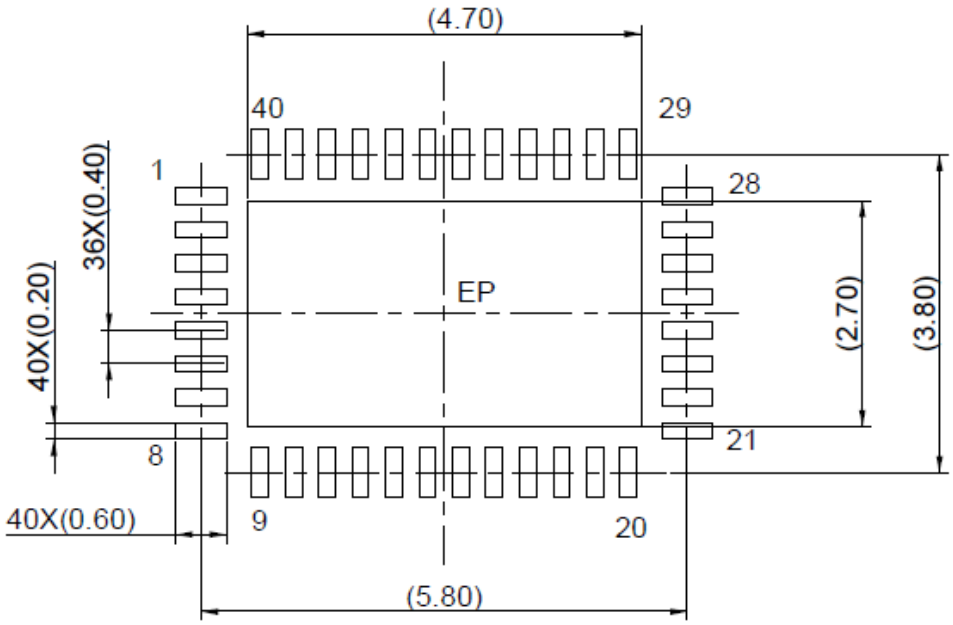


	SYMBOL	DIMENSION IN MM		
		MIN.	NOM.	MAX.
TOTAL THICKNESS (For Reference Only)	A	0.672	0.766	0.86
Pre-solder (For Reference Only)	A1	0.02	0.05	0.08
SUBSTRATE THICKNESS	A2		0.186	
MOLD THICKNESS	A3		0.53	
BODY SIZE	D		4	
	E		6	
LEAD WIDTH	b	0.15	0.20	0.25
LEAD LENGTH	L	0.20	0.25	0.30
LEAD PITCH	e		0.40	
LEAD COUNT	N		40	
EDGE LEAD CENTER TO CENTER	D1		2.80 BSC.	
	E1		4.40 BSC.	
EXPOSED PAD SIZE	D2	2.60	2.70	2.80
	E2	4.60	4.70	4.80
BODY CENTER TO CONTACT LEAD	SE		0.20 BSC.	
	SD		0.20 BSC.	
JEDEC(REF)			N/A	
PACKAGE EDGE TOLERANCE	aaa		0.10	
MOLD FLATNESS	bbb		0.10	
LEAD OFFSET(PACKAGE)	eee		0.10	
LEAD OFFSET(LEAD)	fff		0.05	

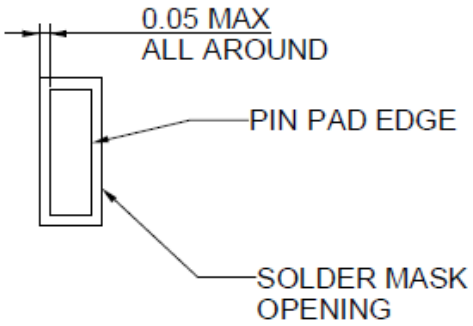
Figure 48: Package Outline of PS7161

9. PCB AND STENCIL GUIDE

9.1 PCB Footprint Example



LAND PATTERN EXAMPLE



SOLDER MASK DETAILS

For Via in pad, it must use resin plugging.

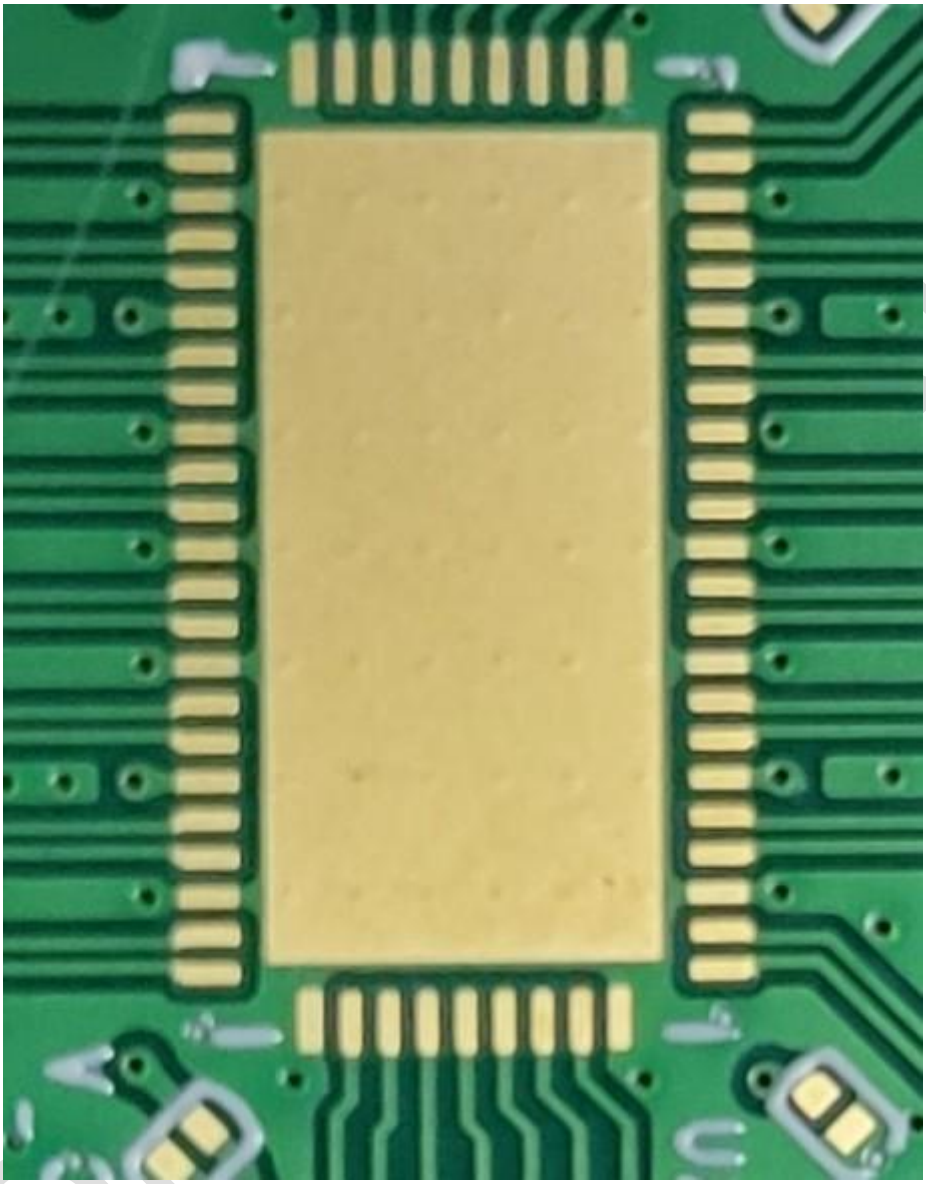
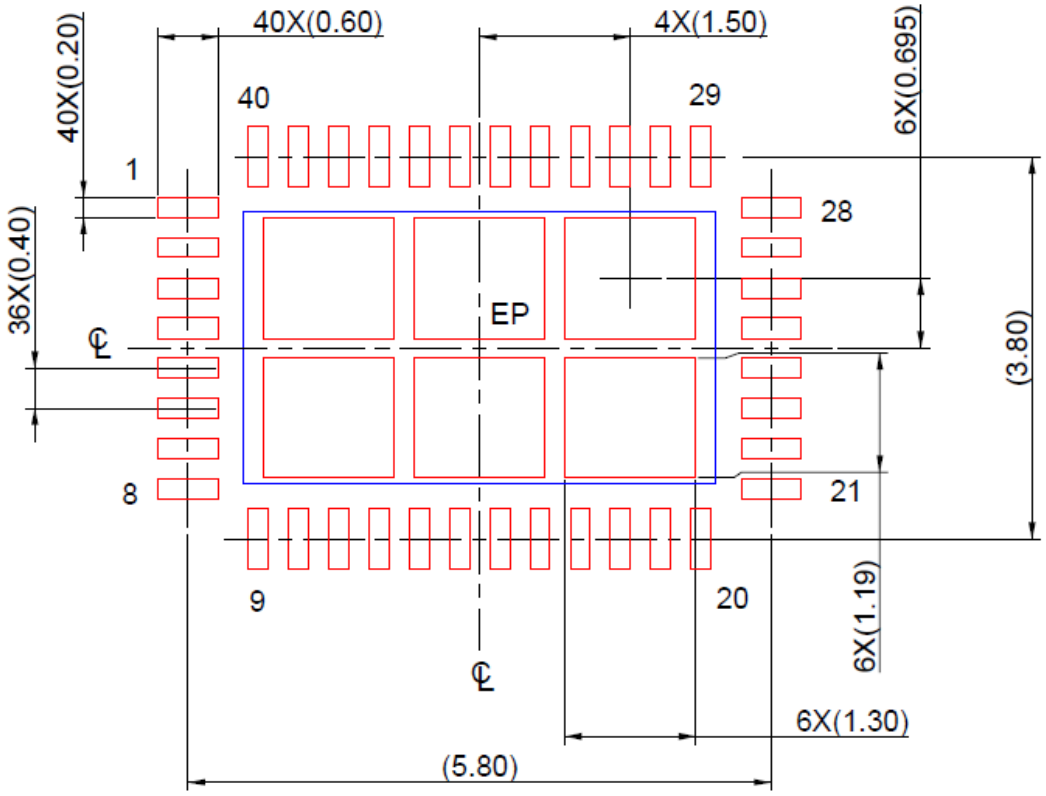


Figure 49: PCB Footprint Example of PS7161

9.2 Stencil Design Example



SOLDER PASTE EXAMPLE

STENCIL THICK: 0.1 MM

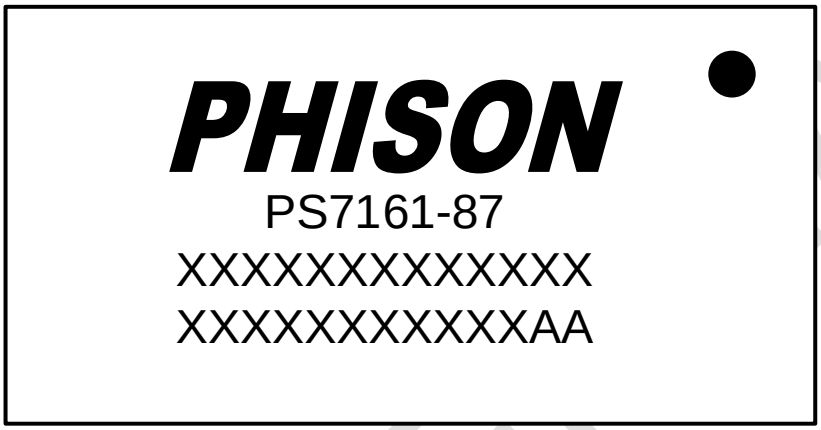
EXPOSED PAD AREA: 73% PRINTED SOLDER COVERAGE

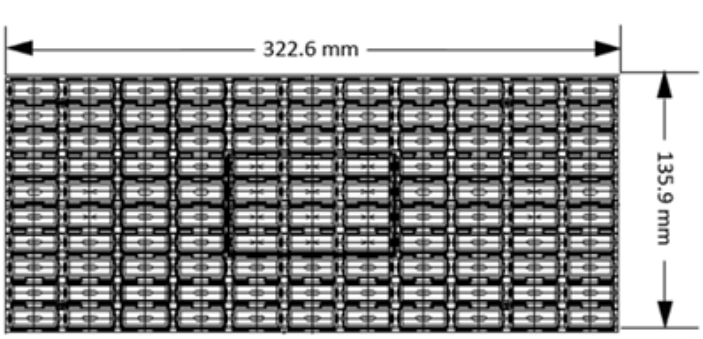
Figure 50: Stencil Design Example of PS7161

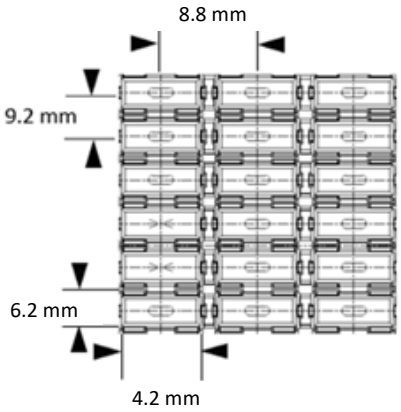
10. ORDERING INFORMATION

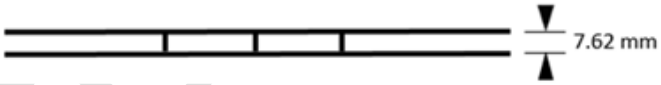
Table 32: Ordering Information

Part Number	Marking	Version	Package Type	Package Size	Packing
PS7161-87	PS7161-87	AA	FC-LGA-40	6.0mm x 4.0mm	Tray









Package	Q'TY/Tray
FC-LGA-40	490