PCI6-AD-x8EDSFF-VE3/VE1/VEQ

User's Manual

REV: 1.0

January. 2025

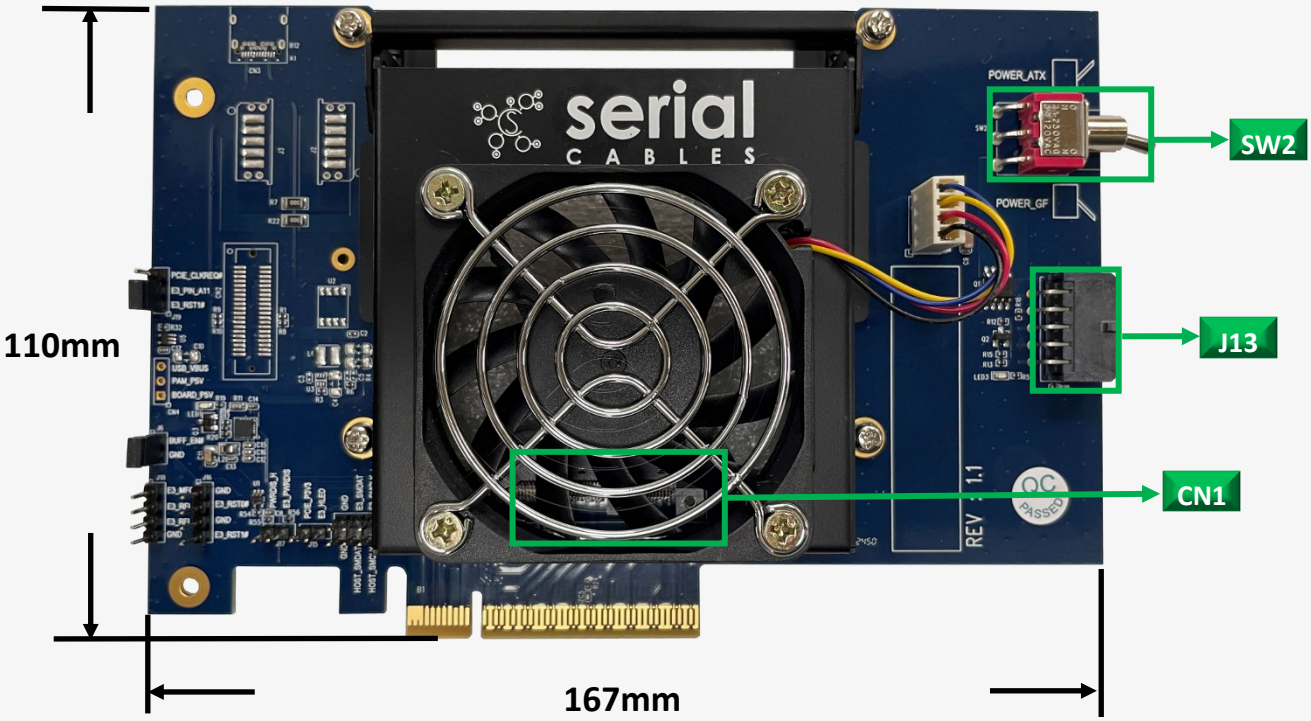
Change history

REV	Change history	Date of Release
1.0	New created	Jan. 2025

Function Description For Connectors

For PCI6-AD-x8EDSFF-VE3 And

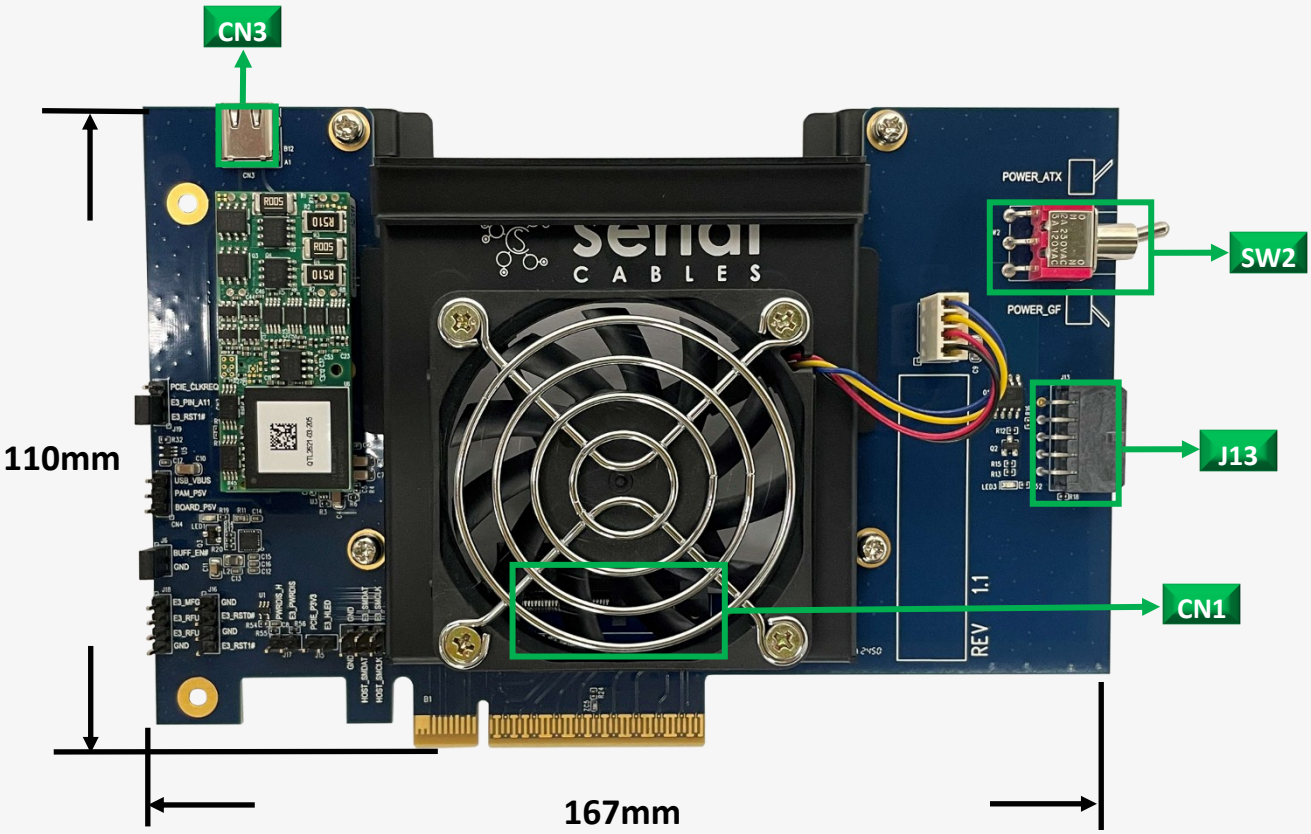
PCI6-AD-x8EDSFF-VE1



Connectors	Descriptions
SW2	Toggle switch Toward Up, EDSFF drive powered by ATX (Quarch PPM connector in). Toward Down, EDSFF drive powered by host (Golden finger).
J13	Quarch power connector
CN1	X8 84Pins Right angle EDSFF Connectors

Function Description For Connectors

For PCI6-AD-x8EDSFF-VEQ



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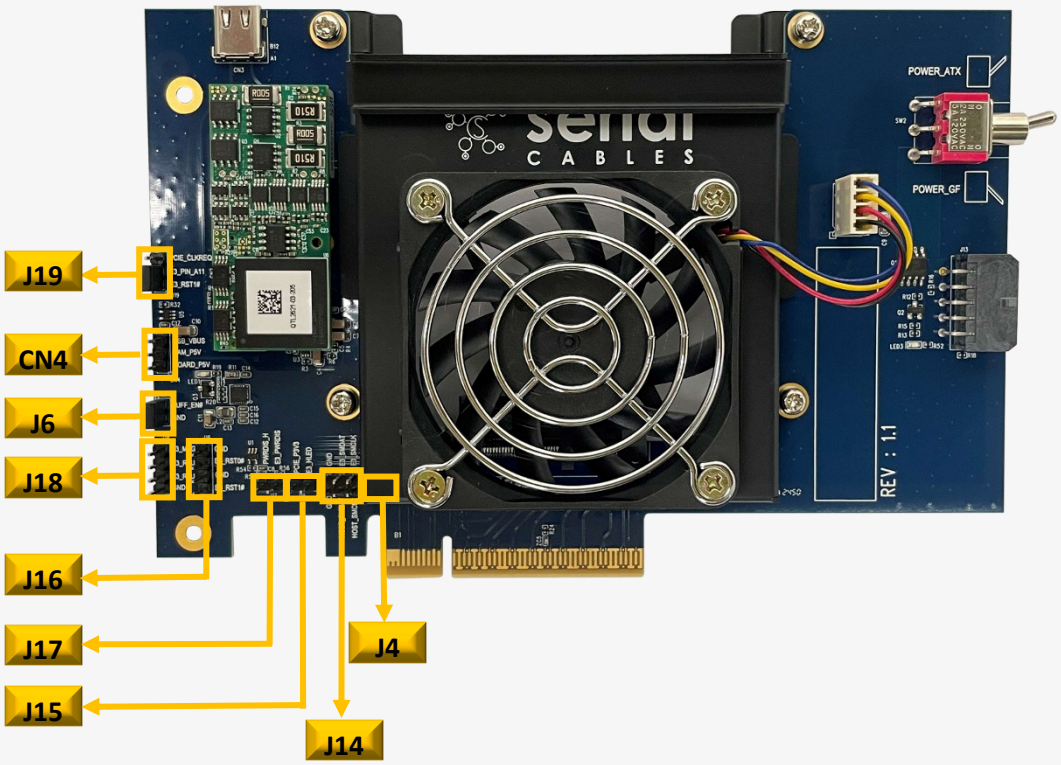
SW2	Toggle switch Toward Up, EDSFF drive powered by ATX (Quarch PPM connector in). Toward Down, EDSFF drive powered by host (Golden finger).
J13	Quarch power connector
CN1	X8 84Pins Right angle EDSFF Connectors
CN3	Type C USB connector

Function Description For Headers



<table>
<tr><th>Headers</th><th>Descriptions</th></tr>
<tr><td>J19</td><td>Select the Pin11 of EDSFF connected to PCIE_CLKREQ# or PERST#.
1.) Jumper on Pin1&2. support single port in EDSFF also connect the CLKREQ# signal from host to EDSFF device.
2.) Jumper on Pin2&3. support dual port in EDSFF also connect PERST#
<table>
<tr><th>Pins in Header</th><th>Signals</th><th>Pins in EDSFF/ Golden finger</th></tr>
<tr><td>3</td><td>PCIE_CLKREQ#</td><td>GF_P12</td></tr>
<tr><td>2</td><td>EDSFF_P11</td><td>EDSFF_A11</td></tr>
<tr><td>1</td><td>EDSFF_PERST1#</td><td></td></tr>
</table></td></tr>
<tr><td>CN4</td><td>Support in “VEQ” SKU only.
it is used to select PAM_P5V come from USB connector or on-board power regulator.
1.) Jumper on Pin1&2. PAM_P5V comes from USB connector.
2.)Jumper on Pin2&3. PAM_P5V comes from on-board power regulator.
<table>
<tr><th>Pins in Header</th><th>Signals</th></tr>
<tr><td>3</td><td>USB_VBUS</td></tr>
<tr><td>2</td><td>PAM_P5V</td></tr>
<tr><td>1</td><td>P5V</td></tr>
</table></td></tr>
<tr><td>J6</td><td>Disable or enable clock buffer output to EDSFF connector.
1.) Jumper ON. Clock buffer outputs HCSL clock to EDSFF connector.
2.) Jumper OFF. Disable clock buffer output.
<table>
<tr><th>Pins in Header</th><th>Signals</th></tr>
<tr><td>1</td><td>BUFF_OE#</td></tr>
<tr><td>2</td><td>GND</td></tr>
</table></td></tr>
<tr><td>J18</td><td>J18 is used for MFG and FRU signals level check
<table>
<tr><th>Pins in Header</th><th>Signals</th><th>Pins in EDSFF</th></tr>
<tr><td>1</td><td>EDSFF_MFG</td><td>EDSFF_B7</td></tr>
<tr><td>2</td><td>EDSFF_FRU</td><td>EDSFF_B8</td></tr>
<tr><td>3</td><td>EDSFF_FRU1</td><td>EDSFF_A42</td></tr>
<tr><td>4</td><td>GND</td><td></td></tr>
</table></td></tr>
</table>

Function Description For Headers (cont.)

<table>
<tr><th>Headers</th><th>Descriptions</th></tr>
<tr><td>J16</td><td>J16 is used for EDSFF PERST# manual reset.

Note: EDSFF PERST1# support in dual port only.

J19 pin2 and pin3 must be short to connect PERST1# to EDSFF Pin A11.
<table>
<tr><th>Pins in Header</th><th>Signals</th><th>Pins in EDSFF</th></tr>
<tr><td>1</td><td>GND</td><td></td></tr>
<tr><td>2</td><td>EDSFF_PERST0#</td><td>EDSFF_B10</td></tr>
<tr><td>3</td><td>GND</td><td></td></tr>
<tr><td>4</td><td>EDSFF_P11</td><td>EDSFF_A11</td></tr>
</table></td></tr>
<tr><td>J17</td><td>J17 is for EDSFF PWRDIS setting.

1.) Jumper ON. Set EDSFF PWRDIS to be “H” level.

2.) Jumper OFF. Set EDSFF PWRDIS to be “L” level.
<table>
<tr><td>Pins in EDSFF</td><td></td><td>EDSFF_B12</td></tr>
<tr><td>Signals</td><td>PWRDIS_H</td><td>EDSFF_PWRDIS</td></tr>
<tr><td>Pins in Header</td><td>1</td><td>2</td></tr>
</table></td></tr>
<tr><td>J15</td><td>J15 is for EDSFF HLED control.

1.) Jumper ON. Connect HLED to P3V3.

2.) Jumper OFF. No connect in HLED.
<table>
<tr><td>Pins in EDSFF</td><td></td><td>EDSFF_A10</td></tr>
<tr><td>Signals</td><td>PCIE_P3V3</td><td>EDSFF_HLED</td></tr>
<tr><td>Pins in Header</td><td>1</td><td>2</td></tr>
</table></td></tr>
<tr><td>J14</td><td>J14 is for EDSFF SMBus accessing.

Pin1&2, Pin3&4 ON: connect the SMBus of EDSFF to host in pins of golden finger.

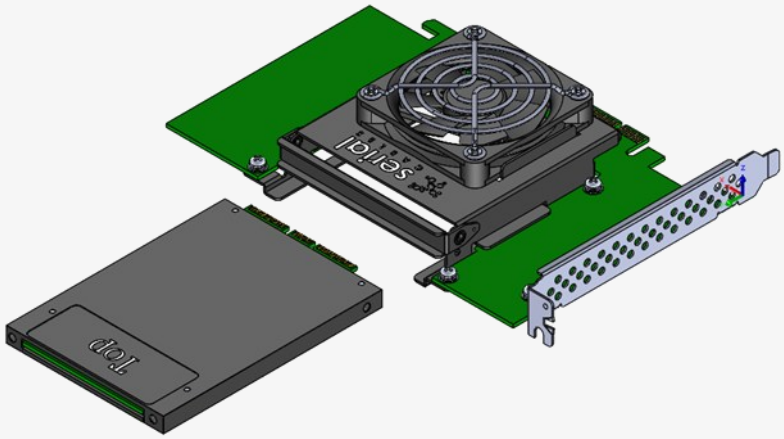
Or SMBus accessing from external I2C analyzer via pins 1, 3 and 5.
<table>
<tr><td>Pins in EDSFF</td><td></td><td>GF_B6</td><td>GF_B5</td></tr>
<tr><td>Signals</td><td>GND</td><td>HOST_SMDAT</td><td>HOST_SMCLK</td></tr>
<tr><td>Pins in Header</td><td>6</td><td>4</td><td>2</td></tr>
</table>
<table>
<tr><td>Pins in EDSFF</td><td></td><td>EDSFF_A8</td><td>EDSFF_A7</td></tr>
<tr><td>Signals</td><td>GND</td><td>EDSFF_SMDAT</td><td>EDSFF_SMCLK</td></tr>
<tr><td>Pins in Header</td><td>5</td><td>3</td><td>1</td></tr>
</table></td></tr>
<tr><td>J4</td><td>J4 is used to set dual port enable/disable in EDSFF.

1.) Jumper ON. Set EDSFF to support dual port.

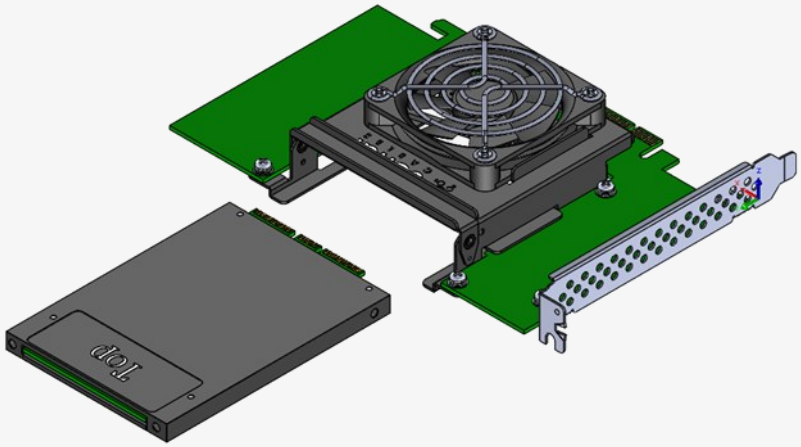
2.) Jumper OFF. Set EDSFF to support single port.
<table>
<tr><th>Pins in Header</th><th>Signals</th></tr>
<tr><td>1</td><td>EDSFF_DPEN#</td></tr>
<tr><td>2</td><td>GND</td></tr>
</table></td></tr>
</table>

"VE3" FAN-cage for E3 SSDs Installation

Hinge down for 7.5mm height E3 SSD



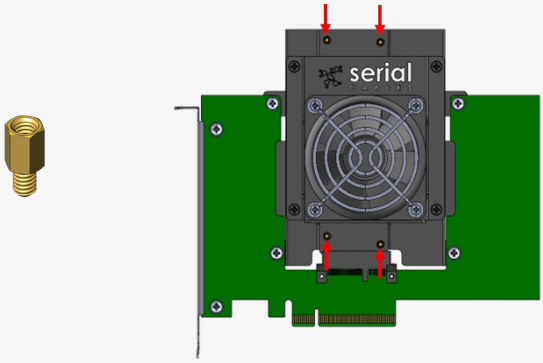
Hinge up for 16.8mm height E3 SSD



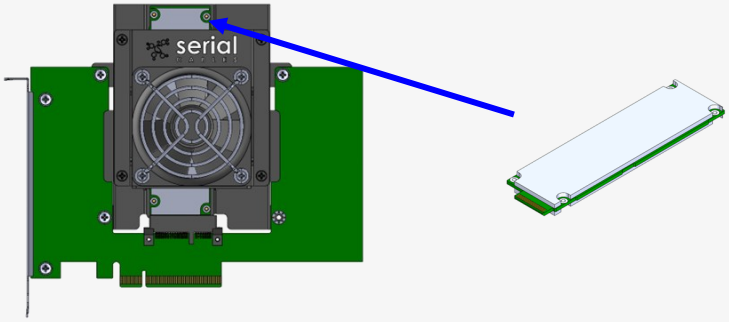
"VE1" FAN-cage for E1.S SSDs Installation

E1S 5.9mm/8.01mm SSDs Installation

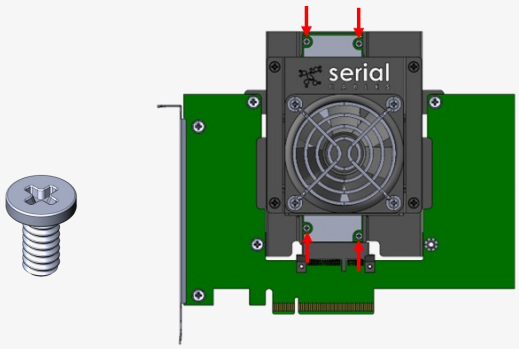
Step1: screw 4pcs of copper pillar onto E1.S FAN-cage



Step2: Install E1.S SSDs.



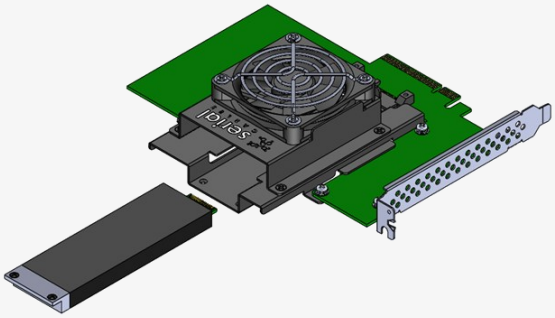
Step3: screw E1.S SSD



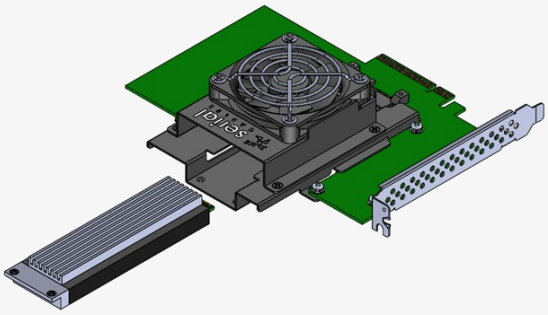
"VE1" FAN-cage for E1.S SSDs Installation

E1S 9.5mm/15mm/25mm SSDs Installation

E1.S 9.5mm SSD



E1.S 15mm SSD



E1.S 25mm SSD