



PCI6-AD-x8E3V-01



User's Manual

REV: 1.0

September. 2024

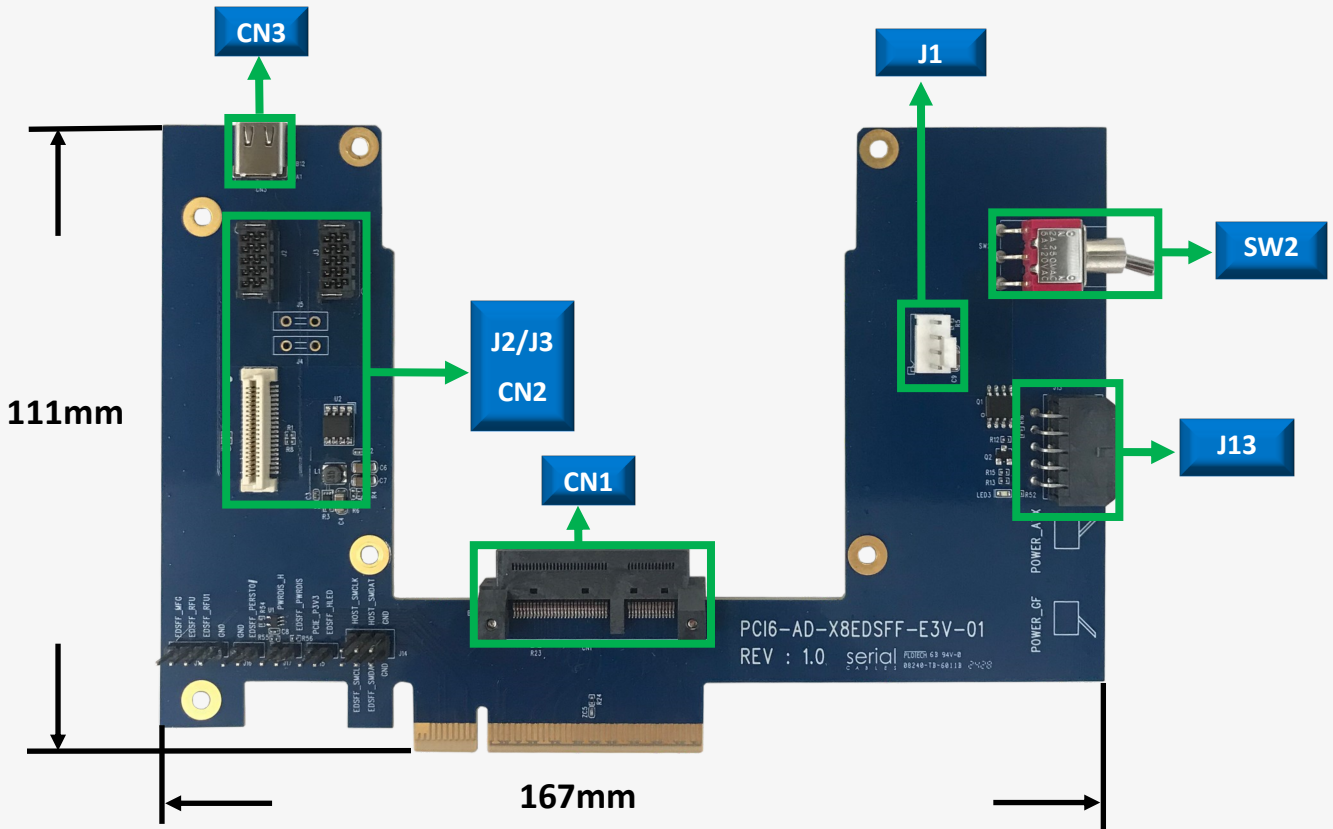


Change history

REV	Change history	Date of Release
1.0	New creation	Sept. 2024



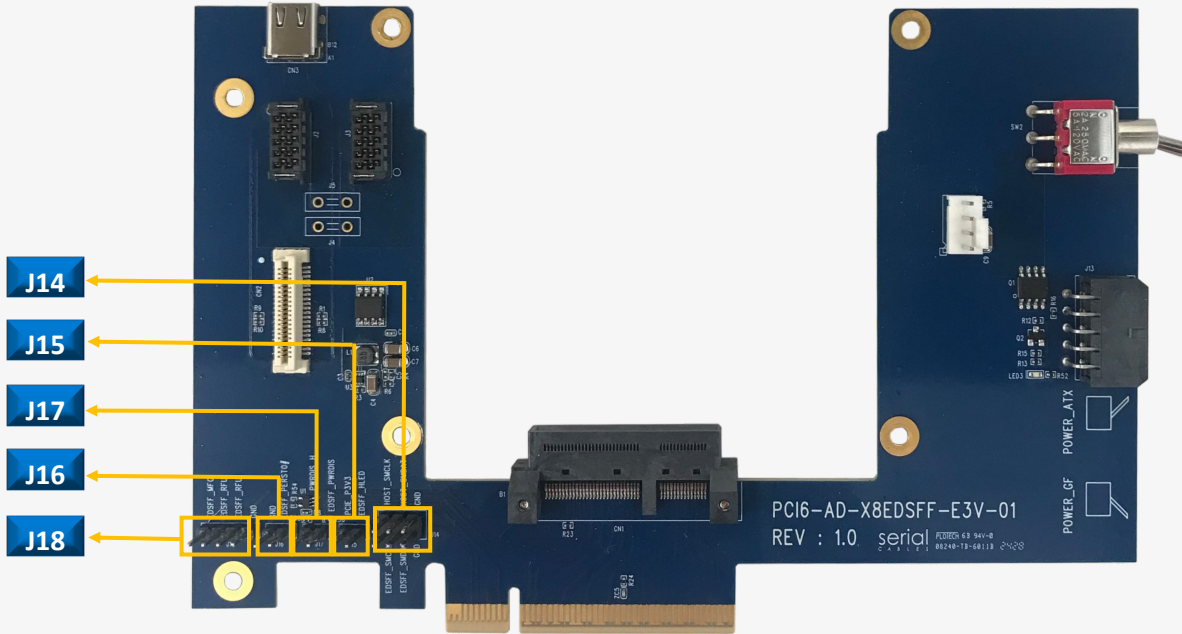
Function Description For Connectors



Location	Descriptions
SW2	Toggle switch Toward Up, EDSFF drive powered by AUX (Quarch PPM Connector). Toward Down, EDSFF drive powered by host (Golden finger).
J13	Quarch PPM connector
J1	4Pins 2.54mm FAN connector
CN1	PCIe Gen6 X8 84Pins Straddle mount EDSFF Connector
CN3	USB Type C connector
J2/J3 CN2	connectors for Shorting board” or “PAM board”



Function Description For Connectors



Location	Descriptions						
J18	<p>Pin1_EDSFF_MFG: To EDSFF connector Pin B7.</p> <p>Pin2_EDSFF_RFU: To EDSFF connector Pin B8.</p> <p>Pin3_EDSFF_RFU1: To EDSFF connector Pin A42.</p> <p>Pin4_GND</p>						
J16	<p>ON: Assert EDSFF_RST# in EDSFF connector Pin B10.</p> <p>OFF: De-assert EDSFF_RST# in EDSFF connector Pin B10.</p>						
J17	<p>ON: Force EDSFF power disable, set PWRDIS in EDSFF connector B12 to "H" state.</p> <p>OFF: Force EDSFF power enable, set PWRDIS in EDSFF connector B12 to "L" state.</p>						
J15	<p>ON: Connects HOST_LED in EDSFF connector Pin A10 to 3.3V.</p> <p>OFF: HOST_LED in EDSFF connector Pin A10 to Floating.</p>						
J14	<p>Jumpers for EDSFF SMBUS accessing</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <tbody> <tr> <td>EDSFF_SMCLK</td> <td>HOST_SMCLK</td> </tr> <tr> <td>EDSFF_SMSDA</td> <td>HOST_SMSDA</td> </tr> <tr> <td>GND</td> <td>GND</td> </tr> </tbody> </table>	EDSFF_SMCLK	HOST_SMCLK	EDSFF_SMSDA	HOST_SMSDA	GND	GND
EDSFF_SMCLK	HOST_SMCLK						
EDSFF_SMSDA	HOST_SMSDA						
GND	GND						